IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al. Defendants.	Civil Action No. 06-726 (JJF) Civil Action No. 07-357 (JJF) CONSOLIDATED CASES

DECLARATION OF DR. MILTIADIS HATALIS IN SUPPORT OF DEFENDANTS CHI MEI OPTOELECTRONICS' PROPOSED CLAIM CONSTRUCTIONS

OF COUNSEL:

Jonathan S. Kagan
Alexander C.D. Giza
Adam Hoffman
Irell & Manella LLP
1800 Avenue of the Stars, Suite 900
Los Angeles, California 90067-4276
(310) 277-1010

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Philip A. Rovner (#3215)
POTTER, ANDERSON & CORROON LLP
Hercules Plaza
1313 N. Market St.
P.O. Box 951
Wilmington, Delaware 19899-0951
(302) 984-6000
provner@potteranderson.com

Attorneys for Defendant
Chi Mei Optoelectronics Corporation

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I, Dr. Miltiadis Hatalis, declare as follows:

I. INTRODUCTION

1. I have been retained as an expert technical witness by Irell & Manella LLP on behalf of Chi Mei Optoelectronics Corporation and Chi Mei Optoelectronics USA (CMO) in connection with the above-captioned action. In this declaration, I provide technical background information relating to U.S. Patent 4,624,737 (the '737 patent, Exhibit B hereto) and 5,825,449 (the '449 patent, Exhibit C hereto) asserted by LG Display Co. Ltd. ("LGD"), and in particular describe certain aspects of fabricating thin film transistors and liquid crystal displays that make use of them. I also provide opinions on the meaning of certain terms used in the '737 and '449 patents to a person of ordinary skill in the relevant art at the time of the respective effective filing dates of the applications for those patents.

2. In preparing this submission, I have studied the '737 and '449 patents as well as their file histories. I have also reviewed the proposed claim constructions set forth in the amended Joint Claim Construction exhibits filed August 6, 2008, for these two patents.

II. QUALIFICATIONS

3. I have studied, taught, and practiced in the relevant flat panel display technology for over 20 years. I received my Doctor of Philosophy (Ph.D.) degree in the field of Electrical and Computer Engineering from Carnegie Mellon University in 1987. The topic of my Ph.D. dissertation research was "Crystallization of Amorphous Silicon Films and its Application in Bipolar and Thin Film Transistors." I received my Masters of Science (M.S.) degree in Electrical and Computer Engineering in 1984 from the State University of New York at Buffalo and my Bachelor of Science (B.S.) degree in Physics in 1982 from the Aristotle University of Thessaloniki in Greece.

4. Upon receiving my Ph.D. degree, I joined the faculty of Lehigh University in the Department of Electrical and Computer Engineering as an Assistant Professor. I was promoted to the rank of Associate Professor with tenure in 1991 and to the rank of Professor in 1995. From 1987-1992, I served as Associate Director of Lehigh's "Microelectronics Research Laboratory." In 1992, I founded and became Director of the "Display Research Laboratory," which was the first academic laboratory in the United States dedicated to research and development of Thin Film Transistors (TFTs) for Active Matrix Liquid Displays (AMLCDs) and Active Matrix Organic Light Emitting Diode (AMOLEDs) displays. As Director of Lehigh's "Display Research Laboratory," I have raised over $10 million through research contracts and grants to support the laboratory's research and development activities on thin film transistors and their application to flat panel displays.

These contracts and grants were awarded by the Defense Advanced Research Program Agency (DARPA), the Army Research Laboratory (ARL), the National Science Foundation (NSF), the National Aeronautics and Space Administration (NASA), the State of Pennsylvania and a variety of industrial companies including IBM, Kodak, Sharp, Northrop Grumman, and others.

5. As a faculty member, I supervised the research of over a dozen Ph.D. dissertations in the technical field of thin film transistors and, along with my graduate students, published over 100 technical publications in scientific journals or conferences in the field of thin film transistors and their application in flat panel displays. In addition to the aforementioned Ph.D. dissertations, I have also supervised a large number of graduate student master's theses and undergraduate projects. I have taught a number of different undergraduate and graduate level courses in the Electrical and Computer Engineering department at the Lehigh University dealing with the physics, technology and the design of solid-state devices and circuits. I have also introduced and regularly teach a course on "Semiconductor Material and Device Characterization," and I have also reorganized a two-course sequence on Design of Very Large Scale Integration (VLSI) which are "Introduction to VLSI Circuits" and "Introduction to VLSI Systems."

6. My research pioneered the low temperature crystallization of amorphous silicon for producing polycrystalline silicon (polysilicon) thin film transistors, as well as the application of these devices to a number of novel circuits for integrated display drivers and their use for fabrication of AMLCD and AMOLED displays. Currently, my research group is investigating the development to flexible displays. We recently presented what we believe to be the world's first VGA flexible Active Matrix Display using polysilicon TFTs.

7. As part of my research, I utilize much of the same equipment and many of the same microfabrication processes that are relevant to the '449 and '737 Patents, including: Plasma Enhanced Chemical Vapor Deposition (PECVD) for intrinsic hydrogenated-amorphous silicon, silicon nitride and silicon dioxide films; sputter and e-beam deposition tools for aluminum, indium-tin-oxide, tantalum and other metallic thin films; photolithographic tools for spinning, exposing and developing photoresist patterns; as well as plasma or wet etching processes for removing various thin film materials from the substrate. I also utilize a variety of electrical characterization techniques and instruments for testing the electrical performance of completed TFT circuits and flat panel displays.

8. As part of my research, I pioneered a technique for crystallizing amorphous silicon. The technique I pioneered has been used in the manufacture of small polysilicon TFT AMLCDs for over a dozen years, and, more recently, polysilicon TFTs have also been used for the manufacture of AMOLED displays. In addition, many industrial and academic laboratories have recently initiated R&D activities related to the fabrication of polysilicon thin film transistors on flexible metal foil substrates and their application to flexible displays. Such research flows from the accomplishments of my research group in this technical field.

9. My industrial experience includes work at the XEROX Palo Alto Research Laboratory and various consulting projects with flat panel display companies as well as companies producing equipment for the manufacture of flat panel displays. All of these projects were related to the thin film transistors and their application to flat panel displays.

10. I am a member of several professional organizations including the Society for Information Displays (SID), and the Electron Device Society of the Institute of Electrical

and Electronics Engineers (IEEE). I have been the chair or co-chair at numerous national and international conferences/symposiums including several SID sponsored Workshops on Active Matrix Liquid Crystal Displays and a Materials Research Society Symposium on Flat Panel Displays. I have co-authored two book chapters, one dealing with the "Polysilicon TFT Technology" and another on application of "Polysilicon TFTs in AMOLED Displays." I have served as a reviewer for technical papers submitted to several scientific journals and have also served as a reviewer for several years for the National Science Foundation Small Business Innovative Research (SBIR) program. My latest curriculum vitae, which includes a list of my publications in scientific journals and conferences, is attached at Exhibit A.

III. CLAIM CONSTRUCTION STANDARDS

11. I understand that in construing patent claims, courts seek to determine what a person of ordinary skill in the art would understand the claims to mean primarily in light of the intrinsic evidence of record, including the written description, the drawings, and the prosecution history. In particular, I understand that the patent specification is considered the single best guide to the meaning of a particular claim term.

12. I also understand that, in general, claim language should be given its ordinary and customary meaning as would be understood by one of ordinary skill in the art at the time of the invention. An exception to this general rule is where a patentee defines his own terms, giving a claim term a different meaning than the term would otherwise possess, or expressly disclaims or disavows the full claim scope. In these situations, the inventor's lexicography governs. Also, the specification may resolve ambiguous claim terms where the ordinary and accustomed meaning of the words used in the claims lacks sufficient clarity to permit the scope of the claim to be ascertained from the words alone.

13. I further understand that when courts look to the specification for clarification of ambiguous claim terms, courts still must avoid reading unclaimed limitations appearing in the specification into the claims. Moreover, I understand that courts may occasionally consider supplemental resources such as dictionaries, encyclopedias, and treatises to assist in determining the ordinary and customary meanings of claim terms.

14. In my opinion, "a person of ordinary skill in the art" for the technology of the '737 and '449 patents would have a Bachelor's of Science degree in Electrical Engineering, Physics (with an emphasis in semiconductors or solid state devices), or Materials Science, and at least several years of experience in the design, development and manufacturing of AMLCD or other types of flat panel displays that utilize thin film transistors, or an equivalent combination of education and work experience.

IV. INTRODUCTION TO THIN FILM TRANSISTORS AND LCD DISPLAYS

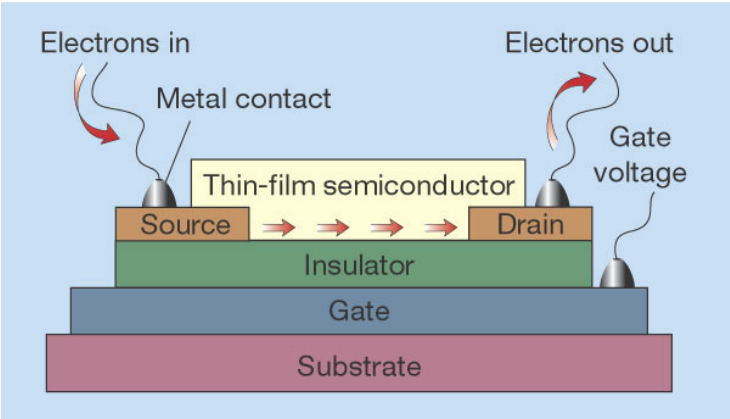
15. Thin-film transistors (TFTs) are the building-blocks of Liquid Crystal Displays (LCD). In a typical LCD, the image is made up of many small elements called pixels, arranged in rows across the display area. The electronic components that control a pixel in a typical LCD include a TFT, a storage capacitor, and a pixel capacitor formed between the pixel electrode and the common display electrode. Both the pixel and the display common electrodes are typically made from a transparent conductive film such an Indium Tin Oxide (ITO). When a voltage is applied to the pixel electrode, the relative rotation of the liquid crystal molecules between the ITO pixel electrode and the common display electrode is affected and this modifies the amount of light that is passing through the pixel.

A. How A TFT Works

16. The TFT serves as a "switch" that controls the amount of voltage to each pixel electrode, which in turn affects the amount of light that passes through each pixel. When turned on, the TFT allows an electrical current to flow into and charge the storage capacitor to a specific voltage. When the TFT is turned off, current cannot flow through it and thus the voltage established at the capacitor is maintained. The voltage stored in the capacitor appears to the pixel electrode, and thereby determines the amount of light that passes through the pixel.

17. The '449 and '737 patents both concern themselves in significant part with the fabrication of TFTs. Therefore, I provide additional background information on the structure, manufacture and operation of TFTs. The following is a simplified conceptual diagram of a generic TFT.

FIGURE A: Conceptual diagram of a common type of TFT



Source: Mercouri G. Kanatzidis, *Semiconductor physics: Quick-set thin films*, Nature 428, 269-271 (March 18, 2004) (Exhibit D hereto).

18. As can be seen in the above simplified diagram, a thin film transistor is an electronic device having three terminals referred to as the "gate," "source" and "drain."

Current flows between the source and drain under control of the gate, through a region referred to as "the channel." More specifically, the current is turned on and off by applying a voltage to the gate. Voltage is applied from an external source to the gate electrode, depicted above generally as the blue region labeled "Gate." The voltage applied to the gate affects the conductive properties of the Thin-film Semiconductor depicted above, which is separated from the gate by an insulating layer (labeled "Insulator"). The thin-film semiconductor is "semi-conductive" – that is, it is neither strictly a conductor nor an insulator, but acts alternatively as a conductor or an insulator depending upon the gate voltage. By controlling the amount of voltage to the gate, the flow of current through the semiconductor between the source and the drain can be controlled. In this way, the TFT can be used as an "on/off" switch.

19. Critical to the operation of the TFT is the aforementioned "channel." The channel in the earlier diagram is the region in the thin-film semiconductor material between the source and drain electrodes and right above the interface with the gate insulator, where electricity is conducted when the TFT is "on." The channel is conceptually depicted in the previous diagram as red arrows from the source to the drain.

B. Structure of a TFT

20. As reflected in the earlier illustration, a TFT is generally built on top of a substrate, usually some kind of insulator such as glass. In a typical process for building such a TFT, the gate electrode is first formed on top of the substrate. The gate electrode is usually a conductor, such as a metal. Next, an insulator is formed on top of the gate electrode. The insulator serves to electrically isolate the gate from the source and drain electrodes and from the thin-film semiconductor containing the channel. Next, a thin-film

semiconductor is formed on top of the insulator. As noted above, the semiconductor can act as a conductor or an insulator, depending on the voltage applied to the gate.

21. Relating the above description to the terminology used in the '737 patent, the function of the Substrate shown in the diagram is generally performed by the "insulating substrate" illustrated in the '737 patent. The function of the Gate in the diagram is generally performed by the "gate electrode" illustrated in the '737 patent. The function of the Insulator in the diagram is generally performed by the "gate insulating film" illustrated in the '737 patent. Finally, the function of the Thin-film Semiconductor in the diagram is generally performed by the "high-resistivity semiconductor film" illustrated in the '737 patent.

22. For thin-film semiconductors made of certain materials, such as undoped hydrogenated amorphous silicon, an extra doped semiconductor layer (not depicted in the conceptual diagram above) may be added between the thin-film semiconductor and the source and drain electrodes to reduce the series resistance between the channel and the source and drain electrodes. The '737 patent refers to such a doped semiconductor layer as a "low-resistivity semiconductor film," which is distinct from the "high-resistivity semiconductor film" in the '737 patent in which the channel is formed.

23. The physics of a TFT defines certain features or characteristics of each of the aforementioned layers. For example, the insulating material between the gate electrode and the thin-film semiconductor will serve both to insulate the gate and control the current through the channel region. The current is modulated through a gate capacitance formed by the gate insulating film. The material used to insulate the gate has a "permittivity," which is a parameter that determines the value of the gate capacitance. The total capacitance of the

insulator film will be a function of the composition of material or materials used, as different materials have different permittivity values, and the total thickness of these materials. An engineering decision on the thickness and composition of the material or materials spanning the region between the upper surface of the gate electrode and the bottom surface of the thin-film semiconductor must be made. In general, for a high performance TFT both a high value capacitance is desired (thinner materials or higher permittivity values result in higher capacitance) and an effective insulation of the gate electrode (thicker materials insulate better).

24. Physics also dictates that the material directly above the gate insulator – i.e., the thin-film semiconductor - will always contain the channel. As noted above, the channel will form in a thin band right above the interface with the insulating film, but does not extend into upper films.

C. Fabrication of a TFT

25. As can be seen from the previous diagram, a TFT device is made from a series of different materials deposited as layers and shaped or patterned into device features. The manufacturing process generally entails the formation of layers from bottom to top. Since a layer is typically deposited over the entire surface, the manufacturing process also generally requires the removal or etching of the layer from certain regions, for example, to expose a portion of the layer underneath or to create desired features having particular geometric shapes. The removal or etching of a layer from certain regions typically requires the use of a "mask," which is made of material that is resistive to a removal or etching technique and generally defines the boundaries of the exposed material to be removed or etched.

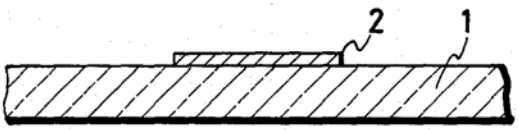
26. During the fabrication process, a device is moved among different tools and machines in order to deposit, clean, etch, and perform other fabrication steps. Deposition or etching of material may occur in a controlled vacuum chamber in order to allow careful control of the process parameters. This allows the process engineer to closely control the deposition rate of the material, for example, or the rate of etching. Between fabrication steps, it may be necessary to move the substrate containing the partially completed devices from one machine (e.g., a vacuum chamber) to another machine. During this time, a device may be generally exposed to the uncontrolled ambient atmosphere, as opposed to the controlled atmosphere within a vacuum chamber or the like. Since the ambient atmosphere contains oxygen and other potential contaminants or impurities, the exposed surfaces of a device may oxidize or collect undesired contaminants or impurities, thus potentially affecting device performance.

V. '737 PATENT

27. The '737 patent describes a particular technique for fabricating a TFT that is said in the patent to use a reduced number of mask steps. '737 Patent, 1:32-53. Another stated goal of this patent is to fabricate the TFT in a manner that minimizes the "channel series resistance." '737 Patent, 4:9-12.

28. The '737 patent compares its fabrication process to a particular prior art process. According to the prior art as described in the '737 patent, a gate electrode 2 is formed on an insulating substrate 1, such as a glass substrate:

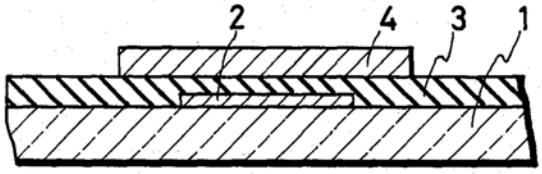
FIG. 1a PRIOR ART



‘737 Patent, 1:12-17. The formation of the gate electrode into the shape of an island is the first masking/etching step described in the prior art sequence.

29. Then, a gate insulating film 3 and an amorphous silicon film 4 are deposited in sequence, and the latter is etched into the shape of an island as shown in Fig. 1b of the ‘737 patent:

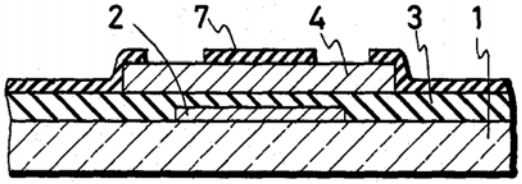
FIG. 1b PRIOR ART



‘737 Patent, 1:17-21. Thus far, the sequence of substrate, gate, insulator, and thin-film semiconductor are the same as shown in the conceptual diagram of a generic TFT depicted earlier. The formation of the thin-film semiconductor into the shape of an island is the second masking/etching step described in the prior art sequence.

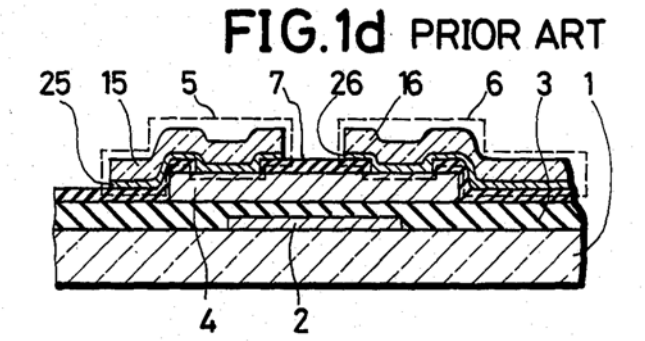
30. Next, an insulating film 7 is deposited, and windows are formed for contact with source and drain regions as shown in Fig. 1c of the ‘737 patent:

FIG. 1c PRIOR ART



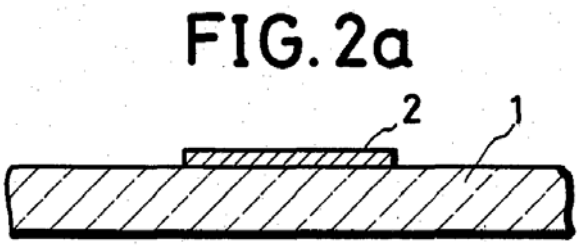
'737 Patent, 1:21-24. The formation of windows in this insulating film is the third masking/etching step described in the prior art sequence.

31. Then, n+ amorphous silicon films 25, 26 and metal (such as Al) films 15, 16 are deposited and selectively etched to form drain and source electrodes 5, 6, thereby resulting in a thin-film transistor as shown in Fig. 1d of the patent below. '737 Patent,1:25-29.



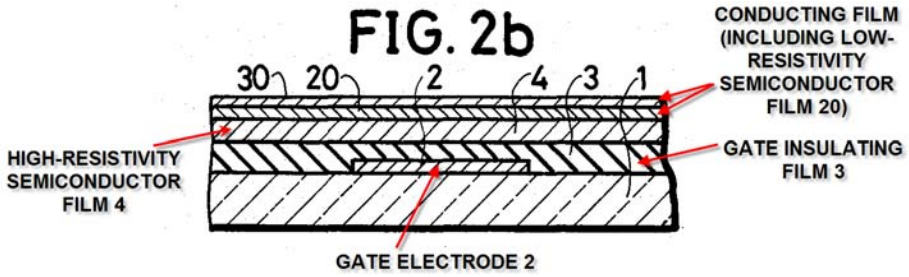
(The n+ amorphous silicon films were not depicted in the earlier conceptual TFT diagram but, as noted above, are sometimes added to facilitate the flow of current between the electrodes and the semiconductor.) The complete removal of the center portion of the metal electrode layer and the doped amorphous silicon layer, electrically isolating the source and drain electrodes, is the fourth masking/etching step described in the prior art sequence illustrated in the '737 patent.

32. The'737 patent purports to reduce the number of masking steps over the prior art depicted in Figs. 1a – 1d. The '737 patent technique is illustrated in Figs. 2a – 2e, and a very similar alternative process is shown in Figs. 3a – 3d. The process starts with the formation of the gate electrode 2 (first masking step) atop an insulating substrate 1 (such as glass, quartz, ceramic, insulator-coated silicon or metal):



'737 Patent, 2:8-14.

33. In a next step, a gate insulating film 3, a high-resistivity film 4, a low-resistivity film 20 and a conducting film 30 are successively deposited on the gate electrode 2 and substrate 1 in a continuous and uninterrupted manner, without exposing them to an oxidizing atmosphere. '737 Patent, 2:17-23. The result is illustrated in Fig. 2b:



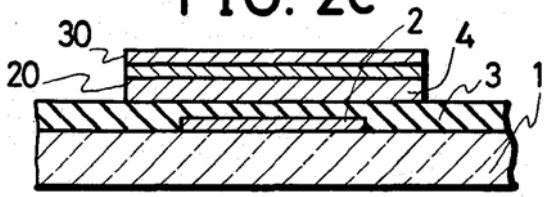
34. Alternatively, the "conducting film" may take the form of a single layer, made up solely of low-resistivity semiconductor film 20. In either case, it is important to the '737 patent that the three films – that is, the gate insulating film 3, high-resistivity semiconductor film 4, and conducting film 20 & 30 – be deposited continuously without exposure to an oxidizing atmosphere, in order to mitigate oxide formation on the interfaces or the collection of impurities and thus avoid an extra electrical resistance between the source and drain and between the channel region. '737 Patent, 1:32-46, 2:17-23. This is achieved by avoiding a masking step between the deposition of the thin-film semiconductor layer and the deposition of the conducting layer, in contrast to the prior art sequence

described above. As explained further below, the continuous deposition of the claimed method allows those layers to be formed without moving the substrate from a deposition chamber to a masking station, thereby exposing it to the ambient atmosphere.

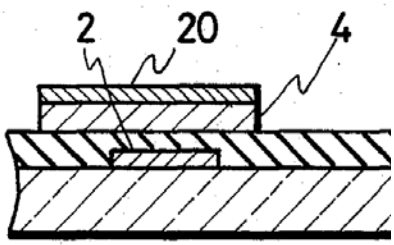
35. To avoid potential confusion, it is worth noting here an inconsistency between the claim language and the language of the specification with regard to the term "conducting film." The specification refers to the conducting film as distinct form the low-resistivity semiconductor film, and identifies them with different reference numerals. For example, the '737 patent refers to "conducting film 30 and low-resistivity amorphous silicon film 20 shown in Figure 2c." '737 Patent, 2:63-64. The claim language, however, requires that the low-resistivity semiconductor film is "contained" within the "conducting film," requiring the conclusion that both 30 and 20 are in fact the "conducting film" as that term is used in claim 1. There is also an alternative embodiment to Figs. 2a – 2e, shown in Figs. 3a – 3d, which is said not to use a conducting film, yet it includes a low-resistivity semiconductor film. While the claim language and specification appear to be inconsistent, I will assume for the present that the "conducting film containing a low resistivity semiconductor film" described in claim 1 also pertains to Figs. 3a – 3d.

36. Following the successive deposition of the three films, in a following step the upper films – i.e., the conducting film (including low-resistivity semiconductor film 20 if applicable) and high-resistivity amorphous silicon film 4 – are etched and left as an island region (second masking step). '737 Patent, 2:54-57. The result is shown in Fig. 2c:

FIG. 2c



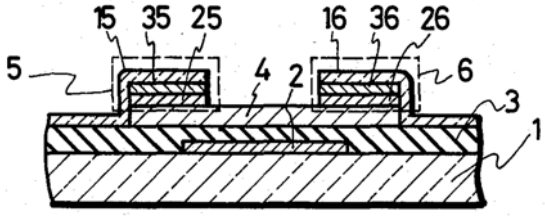
37. Alternatively, the conducting film may take the form of a single layer made up solely of low-resistivity semiconductor 20 as illustrated (after shaping into an island region) in the relevant portion of Fig. 3b reproduced below:



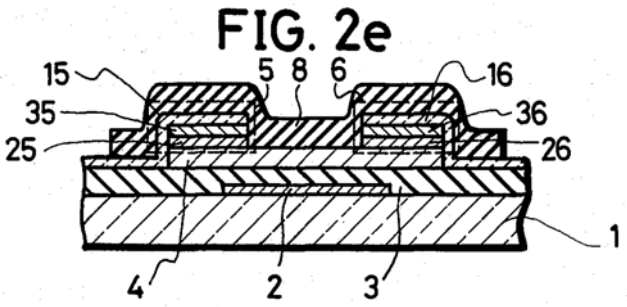
'737 FIG. 3b (Partial View)

38. Next, drain and source electrode members 15, 16 are formed on opposite sides of the island region (third masking step), and the conducting film 30 (including the low-resistivity semiconductor film 20) shown in Fig. 2c are selectively removed with the source and drain electrode members 15, 16 serving as part of the mask to form drain electrode 5 and source electrode 6. '737 Patent, 2:60-66. The result is illustrated in Fig. 2d:

FIG. 2d



39. In a final step, as illustrated in Fig. 2e, a surface passivation film 8 is deposited, and the drain and source electrodes 15, 16 and gate electrode 2 are partly exposed by selective removal of the passivation film 8:



'737 Patent, 3:11-16.

40. Below I will address some of the claim terms that I understand are to be addressed by the Court, and attempt to provide relevant technical or scientific context as well as opinions as to the meaning of particular claim language to one skilled in the art as of the time the '737 patent was filed in the mid-1980's. I attempt to focus on particular areas where CMO's proposed construction differs from the construction of one of the other parties, and do not necessarily intend to address every aspect of each claim construction, particularly where some part of the term does not appear to be in dispute.

41. **Gate insulating film**. As noted above, the gate insulating film in the '737 patent is the first of the three films that are "continuously deposited" atop the substrate 1 and gate electrode 2, as shown in Figure 2b of the patent. The gate insulating film is a thickness of insulating material (such as silicon nitride (SiNx), silicon oxide (SiOx), or a multi-layer film made of such materials) with a high electrical resistance, spanning the region from the gate electrode to the high resistivity semiconductor layer, for insulating the gate electrode from the channel that is formed within the region of the high resistivity semiconductor layer that is right above the gate insulating film.

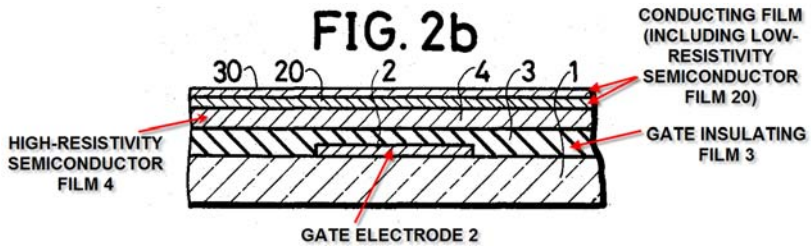
42. The gate insulating film described in the '737 patent is no different from gate insulating films as used in the prior art, and as described in my background explanation earlier for TFTs. That is, the gate insulating film lies between the gate electrode and the high-resistivity semiconductor layer that contains the channel, and serves the purpose of insulating the gate electrode from the channel. To perform this function, the gate insulating film must be of adequate thickness. At the same time, the electrical characteristics of the TFT are closely related to the thickness of the gate insulating material above the gate electrode (the thickness above the substrate is not as relevant, as the channel region is directly above the gate electrode). When the TFT is in the "on" state, the insulating layer must yield proper capacitance such that a channel may be formed. Each material that can be used for a gate-insulating film has a material property known as "permittivity." The total capacitance of the gate insulating film will be a function of the permittivity value of material or materials used and the thickness of these materials. As noted previously, an engineering decision must be made based on a balance of the capacitance and insulating properties of the gate insulating film to determine a thickness of gate insulating film that will produce the desired performance for the TFT. All of the material spanning the region from the top of the gate electrode to the high-resistivity semiconductor layer will impact the insulating properties and the capacitance of this film. Therefore, a person of ordinary skill in the art would understand all of this material to constitute the "gate-insulating film."

43. Accordingly, the term "gate insulating film" in the context of the '737 patent would be understood to mean the entirety of the insulating material that spans the region from the top of the gate electrode to the high-resistivity semiconductor layer.

44. This view is quite consistent with the description and teachings of the '737 patent. For example, the claimed steps of the method itself, as understood by a person of ordinary skill, require a specific location and dimension for the "gate insulating film." The "first step" of Claim 1 initially requires forming a gate electrode on an insulating substrate. The "second step" begins with depositing the "gate insulating film" followed in immediate succession by the "high-resistivity semiconductor film," therefore bounding the gate insulating film between the gate electrode and the high-resistivity semiconductor film.

45. The parties agree that "continuously depositing" means placing the films "without intervening films." This necessarily defines the placement of these three films within the TFT device. In particular, according to the specific order of steps recited in claim 1 and taught in the '737 patent, the "gate insulating film" must span the entire region between the "gate electrode" and the "high-resistivity semiconductor film."

46. The dimension of the gate insulating film is also reflected in Figure 2b, which depicts the gate-insulating film (labeled with the number **3**) as spanning the region from the gate electrode (labeled with the number **2**) and the high resistivity semiconductor layer (labeled with the number **4).**



(annotations added).

As noted previously, the thickness above the substrate depicted to the left and right of the gate is not as relevant, as the channel region is directly above the gate electrode. In those regions to the sides of gate electrode 2, as shown in Fig. 2b, the gate insulating film 3 will generally span from the top of the substrate 1 to the bottom surface of the high-resistivity semiconductor film 4, and would typically be approximately the same thickness as the film above the gate electrode 2 when deposited films such as SiNx or SiOx are used.

47. Furthermore, the '737 patent describes that the "gate insulating film" can be composed of several layers ("Besides SiNx, a film of SiOx *or a multi-layer film made of such materials* can be used as said gate insulating film"). '737 Patent, 2:36-38 (emphasis added). Therefore, however many layers may be deposited between the gate electrode and the high-resistivity semiconductor film, a person of ordinary skill would understand them all collectively to be part of the "gate insulating film."

48. In my opinion, CMO's proposed construction therefore provides the proper meaning of "gate insulating film" in the context of the patent to a person of ordinary skill in the art of thin film transistor manufacture at the time of effective filing date of the '737 patent.

49. CMO's proposed construction also more accurately describes the materials of the "gate insulating film" and its function. With respect to materials, "SiNx, SiOx, or a multi-layer film made of such materials" is taken directly from the patent specification. '737 Patent, 2:36-38. LGD also proposes that the material be "non-conductive" but this definition is too broad in my view, as it might arguably encompass semi-conductors. A better term would be "insulating material." With respect to function of the "gate-insulating film," CMO proposes "insulating the gate electrode from the channel" while LGD proposes

"insulates the transistor gate from the semiconductor." In my opinion, there is little distinction between these constructions, but the CMO construction is preferable because the purpose is to insulate the gate electrode from the channel which is formed within a region of the high resistivity semiconductor located adjacent to the interface of the gate insulating film when the transistor is active ("ON"). The term "channel" here is preferable, in my view, because several semiconductor layers appear in claim 1, and therefore general reference to "the semiconductor" generically could be confusing. The terms "gate electrode" and "transistor gate" appear to be intended to mean similar things, but "gate electrode" more closely follows the claim language and thus would be preferable in my opinion.

50. **High-resistivitity semiconductor film**. The "high-resistivity semiconductor film" is, in the sequence of continuously deposited films, the one that is deposited above the gate insulating film. As explained earlier, in a typical TFT of the type described in the '737 patent, the thin-film semiconductor region between the source and drain acts as the channel. The channel is formed under the influence of the gate voltage and is contained in the region of the high-resistivity semiconductor film adjacent to its bottom surface, i.e., the surface in contact with the gate insulating film. The term "high-resistivity semiconductor film" in the context of '737 claim 1 would therefore be understood by a person of skill in the art to mean a thickness of semiconductor material (such as amorphous silicon or other similar materials) that has a high resistance to current flow and contains the channel formed at the bottom surface of that layer.

51. The term "high-resistivity semiconductor film" in the context of the '737 patent is intimately tied to the function and operation of the channel. As discussed above, a "channel" is an indispensable feature of a thin-film transistor. Moreover, one of the main

goals of the '737 patent is to improve the electrical characteristics of a transistor by reducing "channel series resistance." '737 Patent, 4:9-12. "Channel series resistance" is the total resistance to electric current between the source and drain electrodes that is in series with the TFT channel resistance. The channel series resistance may include, for example, such things as contact resistance, the resistance of the low-resistivity semiconductor film, as well as resistances arising from oxides or other impurities collecting on the interfaces between layers. One alleged difference between the prior art and the process described in the '737 patent is that certain layers, including the channel layer (i.e., high-resistivity semiconductor film), are deposited without exposure to an oxidizing atmosphere. When a layer is exposed to the atmosphere, oxides can be formed or other impurities collected on its surface. '737 Patent, 1:32-40. These can contribute to increased resistance to flow of electrons between the layer below and the layer above. The '737 patent's intended benefit of reduced exposure to an oxidizing atmosphere, therefore, is to lower channel series resistance.

52. The "high resistivity film" in Claim 1 must act as the channel. The physics of this type of thin film transistor dictates that the layer that interfaces with the gate insulator will always contain the channel. In the '737 patent, the high resistivity film is "continuously deposited" over the gate insulator (i.e., the "gate-insulating film"). Therefore, it must necessarily act as the channel in this type of device.

53. The depiction of the TFT in the preferred embodiment of the '737 patent supports this conclusion. It states that "the channel areas of the thin-film transistor are safe from damage by cleaning as they are covered with conducting film **30**." Col. 3:2-4. As noted above, the term "conducting film," in the claim, includes both the "conducting film" and the "low resistivity film 20," and from the context, that appears to be how the term is

used here. The layer covered by the conducting film is the high-resistivity semiconductor film.

54. Besides the points discussed above, CMO's construction also correctly specifies that the "high-resistivity film" must in fact have high resistance, not just "higher" resistance than some other layer. If the "high resistivity film" was in fact a material with low resistance that just happened to be marginally higher than the "low resistivity film," the TFT would not work as intended. For example, the TFT would have high leakage current, meaning that current could flow between the source and drain even without voltage applied from the gate. The resistivity of the "high-resistivity film" must be high enough for the transistor to work as intended, not simply higher than that of the low-resistivity film.

55. **Without exposing … to an oxidizing atmosphere.** The '737 patent requires that the gate insulating film, high-resistivity semiconductor film, and conducting film must be deposited "without exposing them to an oxidizing atmosphere." This means that these films must be deposited without permitting them to come into contact with an uncontrolled ambient atmosphere which contains oxidizing agents.

56. As described earlier, the manufacturing process of TFTs include the use of various deposition chambers in order to deposit films, as well as other tools. These deposition chambers are usually a controlled environment where gases are injected and combined, and the resulting reactions cause layers to be deposited on a surface (the substrate or a previous layer). The manufacturing process also includes other steps, such as cleaning, masking, etching, and so forth. Typically, in the manufacturing processes in use at the time the '737 patent was filed, when samples were moved from one station (such as a deposition chamber) to another (such as a lithography tool for masking), they would be exposed to an

ambient atmosphere. Oxygen and its compounds (such as water vapor) found in the ambient atmosphere can cause undesirable oxidation of certain materials. The sample could also be exposed to other undesirable impurities, particles or other contaminants in the ambient atmosphere. The manufacturing process must therefore be carefully planned so that samples would be moved between stations at times that minimize undesirable exposure to the uncontrolled atmosphere (for example, when none of the exposed surface is particularly sensitive to oxidation and other contaminants).

57. The alleged innovation of the '737 patent is a process of depositing layers of a TFT that minimizes the oxidation or collection of contaminants or impurities at the interfaces between the gate-insulating film, high-resistivity semiconducting film, and low-resistivity semiconducting film. In describing the prior art, the specification states "since the masking step precedes the deposition of n+ amorphous films 25, 26, natural oxide is produced on the exposed surface of amorphous silicon film **4.** Although such natural oxide can be removed… the possibility is still great that oxygen and its compounds as well as other impurities can collect on the laminate surface as it is exposed to the atmosphere." '737 col. 1:33-40. A person of ordinary skill in the art would have understood that "***the atmosphere***" in this context refers to the uncontrolled ambient atmosphere that will be encountered in an ordinary manufacturing process when a sample is moved between the lithography tool for "the masking step" and the chamber used for the "deposition of n+ amorphous films." Between these two process steps, exposing the sample to the ambient atmosphere, which contains oxygen and its compounds (like water vapor) as well as other possible contaminants, could lead to formation of oxides or collection of other impurities on the laminate surface of the sample.

58. As an alternative and alleged improvement to the prior art technique described above, the patent describes the "continuous deposition" of the gate insulating film, high-resistivity semiconductor film and conducting film, without a masking or other operation between these deposition steps. The patent requires that this "continuous deposition" of these layers take place "without exposing them to an oxidizing atmosphere." Based on the patent's comparison of the claimed process with the prior art of Figs. 1a – 1d, a person of skill would also have understood that the claimed step of avoiding exposure to an oxidizing atmosphere refers to the uncontrolled ambient atmosphere that would be encountered between the deposition chamber and another station, such as a lithography tool or cleaning tool. The description at column 2, lines 17-53 of the '737 patent relating to this part of the fabrication process indicates that all of the relevant films would be deposited using the same tool (either in the same chamber or "in-line" chambers adjacent to each other within the same tool – see 2:30-36), thus avoiding the need to transfer the partially completed sample between different tools, which would expose it to the outside ambient atmosphere including its oxidizing agents and contaminants.

59. This point is emphasized again at column 2, lines 33-36 of the '737 patent, which states in connection with successive deposition of the relevant films: "Further, when a sputtering or metalizing chamber is additionally provided, conducting film 30 can also be deposited continuously without exposure to the atmosphere." The '737 patent explains here that the addition of another (e.g., in-line) chamber in the depositing station avoids the need to transfer the sample between tools, which would expose it to "the atmosphere" (that is, the outside ambient atmosphere). In other words, the '737 patent equates "an oxidizing atmosphere" with "the atmosphere" (i.e, the ambient atmosphere), and tends to use these terms in an interchangeable fashion.

60. The fact that those skilled in the art would understand reference to "the atmosphere" in the '737 patent to mean the outside or uncontrolled ambient atmosphere is further reflected by contemporaneous U.S. Patent No. 4,343,081 (the '081 patent, Exhibit E hereto) issued in August 1982 to Francois Morin et al. That patent is directed to essentially the same problem as the '737 patent, including making a thin film transistor (TFT) by successively depositing various films (semiconductor, insulator and metal) while avoiding contamination (or "pollution") at the relevant interface(s). See '081 Patent at col. 1:29-33, 2:4-9. The '081 patent explains that such contamination can be avoided by forming all of the layers "in vacuo" (that is, in conditions of a vacuum chamber) and "in one manufacturing cycle." Id., 1:29-33, 2:4-9. In other words, the various films are formed "successively" and "without contact with the outside atmosphere." Id., 2:33-40, Abstract. The '081 patent uses the terminology "outside atmosphere" (that is, the uncontrolled ambient atmosphere) to refer to what the '737 patent refers to simply as "the atmosphere," but in both cases they mean the same thing: the films should be successively deposited using the same tool while preventing contact with the uncontrolled ambient atmosphere.

61. Therefore, in my opinion, CMO's proposed construction provides the proper meaning of "without exposing them to an oxidizing atmosphere" in the context of the '737 patent to a person of ordinary skill in the art of thin film transistor manufacture at the time of effective filing date of the '737 patent.

62. The alternative construction offered by LGD, which focuses on the outcome rather than the process itself, is vague in my view. The LGD proposal requires that the result is an interface without a "detectable amount of oxidation." First, the term "detectable" is not easily applied because it would be highly dependent on the detection

technology used. There are technologies available that can detect extremely small amounts of oxidation. XPS (x-ray photoelectron spectroscopy), TEM (transmission electron microscopy), SEM (scanning electron microscopy) and other techniques can be applied to detect minute amounts of oxides in structures. In addition, remarkable advances in characterization techniques are continually being realized at the nano- and the atomic scales. It is unclear which of these techniques would be applicable when determining whether an oxide is "detectable." Also, the LGD proposal focuses only on oxide detection, whereas '737 patent is concerned about other impurities from the atmosphere. See '737 patent 1:35-40 ("Although such natural oxide can be removed by an aqueous solution of hydrofluoric acid (HF) or a similar substance, the possibility is still great that oxygen and its compounds ***as well as other impurities*** can collect on the laminate surface ***as it is exposed to the atmosphere***."). In fact, the above quoted text suggests that because there was already a known solution in the prior art for dealing with oxide formation, if anything the '737 patent was possibly more concerned about other impurities or contaminants forming on the interfaces, but these concerns are absent from LGD's proposed construction.

63. **Selectively removing said conducting film exposed on said island region.**

After the various films discussed earlier are "continuously deposited," the process described in Claim 1 requires etching the semiconductor film and conducting film into an "island region", adding a source and drain electrode on either side of the island region, and then "**selectively removing said conducting film exposed on said island region."** This would be understood by one skilled in the art to mean the act of eliminating all the exposed conducting film in the space between the edges of the source and drain electrodes.

64. When those skilled in the art of semiconductor processing refer to "removing" a layer or film, what is meant is removing the entirety of the layer or film that is exposed to the removal process. This is how the term "removal" would be understood in the context of the '737 patent.

65. This understanding is also reflected in the '737 patent text and illustrations, which shows the entirety of the conducting film exposed between the source and drain electrodes as being "removed." This process is shown graphically, for example, in the sequence of steps in Figures 2c and 2d of the '737 patent. (An analogous process is also depicted in the sequence of '737 Figs. 3b and 3c). For clarity of illustration, I have added below a figure to the series of figures in the patent, which I have designated figure 2d' representing the acts described in the specification but not illustrated. To repeat my earlier explanation, Figure 2c is the result of etching the top layers of the TFT, leaving an "island" consisting of the conducting film **30,** the low-resistivity amorphous silicon film **20** and the high-resistivity amorphous silicon film **4**. 2:54, 57. The next step, described but not depicted, is that drain and source electrodes are added over each end of the island region. 2:60-62. This step is depicted below in Fig. 2d' (modified). Finally, "conducting film **30** and low-resistivity amorphous silicon film **20** are selectively removed," as depicted in figure 2d. As can be seen from the figure, *all* of the conducting film in the space between the edges of the source and drain electrodes is removed.

FIG. 2c

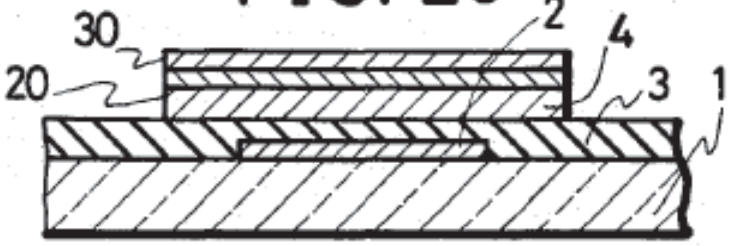


Fig. 2d'
(modified)

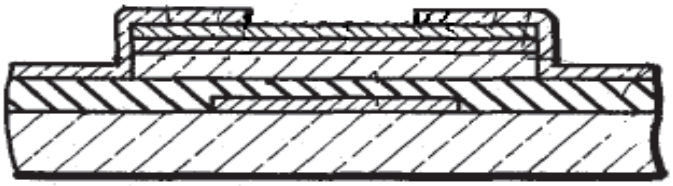
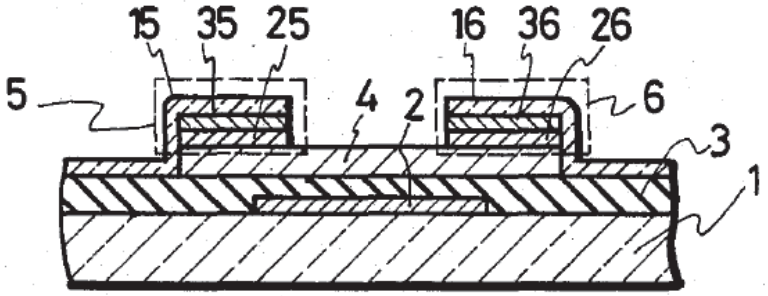


FIG. 2d



66. It is particularly important that the conducting layers (depicted here as **20** and **30**) are fully removed. If a small amount of layer 20 remains, there would be a risk that the TFT would be subject to shorting and not work properly. In fact, the '737 patent recommends over-etching to ensure complete removal of the conducting film and avoid this type of failure. '737 Patent, 3:7-10. This confirms my view that the '737 patent intended "selectively removing" the exposed film to mean eliminating all of the exposed film.

67. The context of the claim also supports this construction. The claim requires that the source and drain electrodes serve as at least part of the mask for this removal step. A mask is made of material that is resistive to a removal technique and defines by its edges the boundaries of the exposed material selected for removal. Therefore, since the source and drain electrodes are serving as a part of the mask in connection with the selective removal step, the profile of the exposed material removed must match the positions of the source and drain electrodes, as depicted in figure 2d.

68. In my opinion, CMO's proposed construction provides the proper meaning of "selectively removing said conducting film exposed on said island region" in the context of the '737 patent to a person of ordinary skill in the art.

VI. THE '449 PATENT

69. The '449 patent describes a technique for forming a wire structure for an LCD array. As described earlier, a TFT can be used as an "on/off switch" for controlling the state of a pixel on an LCD display. Each TFT needs to be electrically connected to external components in order to operate. These external components supply electrical signals which eventually interact with the source and the gate electrodes. The signals are brought to the pixel by metal lines. Lines that supply the signal to the source electrodes are known as Data Lines, and lines supply the signal to the gate electrode are called Gate Lines. The electrodes of the TFT and the metal lines are often times not electrically connected until the later steps in the manufacturing process. Often times these conducting structures are separated laterally and/or vertically by one or more insulating layers. In order to electrically connect these structures, small openings are etched completely through the insulating material to expose the conductive layers beneath. These openings are sometimes referred to as contact holes or

vias. After these openings are created, conductive material is deposited to fill the contact holes or vias and form parts of the wiring structures necessary to electrically connect the conductive layers beneath the insulating material.

70. An example of a process in which contact holes are used to expose underlying conductive layers so that they can be electrically connected by additional conductive material is illustrated in Figs. 1a – 1e of the '449 patent (by contrast, Fig. 3 only shows the end result of such a process). The process of Figs. 1a – 1e is said in the '449 patent to be Prior Art. First, Figure 1a illustrates the deposit of a conductive layer on a transparent glass substrate 1, followed by patterning to form features such as a source pad 2A, gate electrode 2, storage capacitor 20 and a gate pad 2B ('449 Patent, 1:34-39):

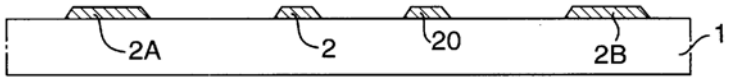


FIG. 1a
PRIOR ART

71. Next, as shown in Fig. 1b, a gate insulating film is formed over the entire surface of the substrate, followed by the formation of an island of amorphous silicon 4 and a doped semiconductor layer 5 over the gate electrode 2 ('449 Patent, 1:40-50):

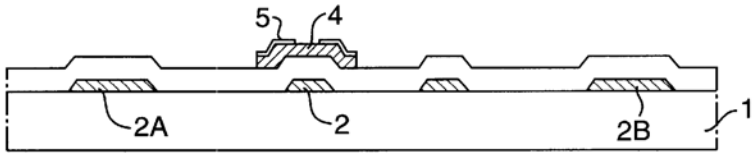


FIG. 1b
PRIOR ART

72. Then, as shown in Fig. 1c, the gate insulating film 3 is selectively etched to expose the source pad 2A and gate pad 2B, in order to enable communicate information from an external driving circuit to the gate and source (‘449 Patent, 1:52-55). The selective etching results in contact holes exposing the source pad 2A and gate pad 2B:

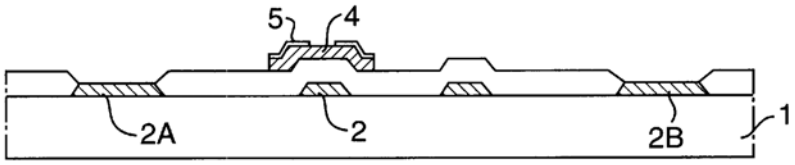


FIG. 1c
PRIOR ART

73. Next, as shown in Fig. 1d, a transparent conductive layer such as Indium Tin Oxide (ITO) is deposited on the entire surface and patterned to form, among other things, patterns 6A on the source pad 2A and gate pad 2B, respectively (‘449 Patent, 1:56-60, although the patent text erroneously refers to “6B” above the gate pad, suggesting that the label in the figure over 2B should actually be “6B”)):

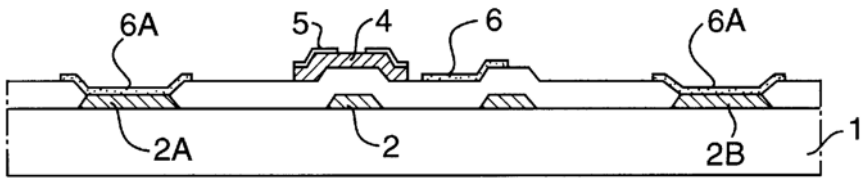


FIG. 1d
PRIOR ART

74. As shown next in Fig. 1e, the TFT is formed on the active layer and includes a conductive layer deposited on the substrate and simultaneously patterned to form source and drain electrodes 7 and 8, respectively. ‘449 Patent, 1:61-64. As can be seen in Fig. 1e,

the source electrode is connected to source pad 2A through one contact hole, and the drain electrode 8 is in contact with impurity-doped semiconductor layer 5 and pixel electrode 6:

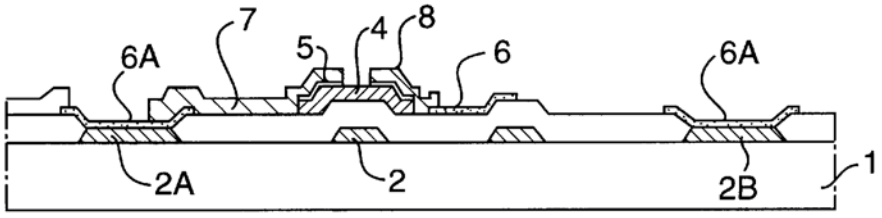
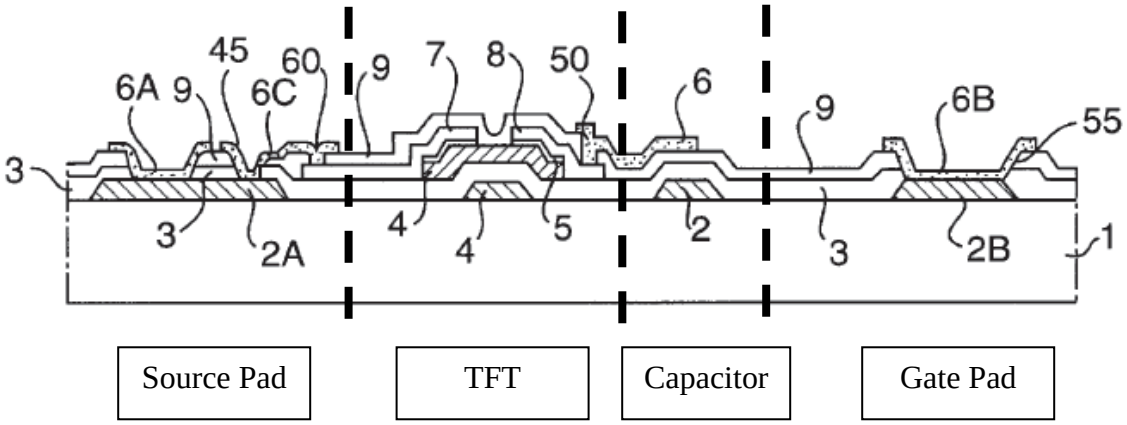


FIG. 1e
PRIOR ART

75. The cross-sectional views illustrated in Figures 1a – 1f, 2a – 2d and 3 of the '449 patent are slightly broader in scope than the cross-sectional views shown in the '737 – in addition to the transistor (TFT), they also include other features such as the storage capacitor, source pad, and gate pad. The capacitor, as discussed before, maintains the voltage at the pixel electrode. The source pad and gate pads connect the transistor to the circuit that drives and controls the display. I have labeled the different general portions of Figure 3 of the '449 patent below for illustration purposes, with the caveat that there is not necessarily a precise dividing point between the regions identified below, at least not as can be identified at this level of illustration.



76. In the following section I will address some of the claim disputes that I understand may be presented to the Court and, as with the '737 Patent, attempt to provide relevant technical or scientific context as well as opinions as to the meaning of particular claim language to one skilled in the art as of the time the '449 patent was filed in the mid-1990's. As before, I do not necessarily intend to address every aspect of each claim construction, but attempt to focus more on particular areas where CMO's proposed construction differs from the construction of one of the other parties.

77. **Conductive layer.** Claim 1 describes a wiring structure with a first "**conductive layer**" and a second "**conductive layer**." In the context of the '449 patent, the term "conductive layer" would be understood by one skilled in the art to mean a single thickness of electrically conductive material that may include one or more patterned features, all of the same uniform material (i.e., single material).

78. In the art of semiconductor manufacture, intended structures are created by initially depositing a layer material that blanket the entire surface, followed by steps to remove the undesired material. The patterns of material left on the surface are the remnants of the initial layer that was deposited. These patterns would naturally share common

material characteristics. In other words, structures that were formed from a common deposition step and subsequent patterning can be thought of as belonging to a common "layer." The simultaneous formation of the patterns/structures is intended to minimize the cost and time in the manufacture of the final product. Therefore "conductive layer" would mean the initial conducting material (such as metals and certain types of oxides, such as indium tin oxide for example) that is deposited according to a given process, as well as the resulting pattern of conducting material after subsequent patterning.

79. This meaning of "conductive layer" is confirmed by the '449 patent specification. With regard to the conductive layer including one or more patterned feature, the '449 specification states, for example, that "a conductive layer is formed on a transparent glass substrate **1** and patterned to form a gate electrode **2**, a storage capacitor electrode **2D**, and a gate pad **2C**, all of the same material." '449 patent at 3:44-47. The specification repeatedly speaks of the "conductive layer" as including various patterned features, as is captured by the language proposed in CMO's construction. '449 Patent, 1:34-37, 1:56-60, 1:61-64, 2:37-46, 3:44-47, 4:64 - 5:1, 5:6-8, 5:16-22. Another example is in the *Summary of the Invention*, which describes that a "gate electrode[,] a gate pad and a source pad [are] formed on the substrate as a first conductive layer." '449 Patent, 2:37-40.[1] Along these same lines, claim 10 of the '449 Patent also illustrates that a conductive layer may include multiple patterned features – specifically, "a gate electrode, a gate pad, and a source pad." '449 Patent, 7:36-39.

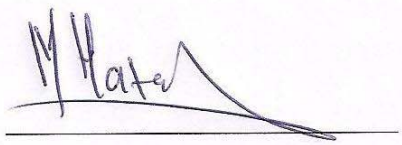
[1] While the '449 patent text in the summary erroneously has a semicolon following "gate electrode" instead of a comma, it is clear that the gate electrode is part of the first conductive layer because of the later description appearing in the detailed description of the embodiments as well as claim 10. *See, e.g.*, '449 Patent, 4:50-52.

80. The ‘449 specification also explains that, since all of the patterned features of a conductive layer are initially deposited at the same time, before patterning, all of the patterned feature are “of the same material” (‘449 Patent, 3:44-47), and this is an inherent characteristic of the patterned features given that they are all deposited at the same time, as part of the same process. The ‘449 patent repeatedly confirms the fact that the patterned features of the conductive layer are all the same material. For example, it states that “***source pad 2A is composed of gate material***, as in the conventional method, and is formed at the same time as gate 2, storage capacitor electrode 2D and gate pad 2B” (‘449 Patent, 4:50-53), and again that “both the first (45) and fourth (60) contact holes are formed over the ***source pad 2A (formed of the same material as the gate***) and source electrode, respectively….” ‘449 Patent, 4:56-59. Likewise, a transparent conductive layer of indium tin oxide (ITO) is deposited and patterned into various features, all of the same uniform material – ITO. See ‘449 Patent, 1:56-60, 5:16-22. There is no instance in which the ‘449 patent describes a conductive layer patterned into features having different materials, and, again, since the conductive material is deposited uniformly over the substrate the patterned features formed from that layer will always share the same uniform composition.

81. In my opinion, CMO’s proposed construction provides the proper meaning of “conducting layer” in the context of the patent to a person of ordinary skill in the art of thin film transistor manufacture at the time of effective filing date of the ‘449 patent.

I declare under the penalty of perjury under the laws of the United States of America and the state of Delaware that the foregoing is true and correct.

Executed on August 11, 2008 in Thessaloniki, Greece.



Dr. Miltiadis Hatalis

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

CERTIFICATE OF SERVICE

I, Philip A. Rovner, hereby certify that on August 11, 2008, the within document was filed with the Clerk of the Court using CM/ECF which will send notification of such filing(s) to the following; that the document was served on the following counsel as indicated; and that the document is available for viewing and downloading from CM/ECF.

BY CM/ECF, HAND DELIVERY AND E-MAIL

Richard E. Kirk, Esq.
Ashley Blake Stitzer, Esq.
The Bayard Firm
222 Delaware Avenue
Suite 900
P.O. Box 25130
Wilmington, DE 19899
rkirk@bayardfirm.com
astitzer@bayardfirm.com

BY CM/ECF, HAND DELIVERY AND E-MAIL

John W. Shaw, Esq.
Karen L. Pascale, Esq.
Young Conaway Stargatt & Taylor LLP
The Brandywine Building
1000 West Street, 17th Floor
Wilmington, DE 19801
jshaw@ycst.com
kpascale@ycst.com

I hereby certify that on August 11, 2008 I have sent by E-mail the foregoing document to the following non-registered participants:

Gaspare J. Bono, Esq.
Matthew T. Bailey, Esq.
Lora A. Brzezynski, Esq.
Cass W. Christenson, Esq.
R. Tyler Goodwyn, IV, Esq.
McKenna Long & Aldridge LLP
1900 K Street, NW
Washington, DC 20006
gbono@mckennalong.com
mbailey@mckennalong.com
lbrzezynski@mckennalong.com
cchristenson@mckennalong.com
tgoodwyn@mckennalong.com

Vincent K. Yip, Esq.
Peter J. Wied, Esq.
Jay C. Chiu, Esq.
Katherine F. Murray, Esq.
Ms. Denise Esparza
Paul Hastings Janofsky & Walker LLP
515 South Flower Street
Los Angeles, CA 90071
vincentyip@paulhastings.com
peterwied@paulhastings.com
jaychiu@paulhastings.com
katherinemurray@paulhastings.com
deniseesparza@paulhastings.com

Ron E. Shulman, Esq.
Julie M. Holloway, Esq.
Wilson Sonsini Goodrich & Rosati
650 Page Mill Road
Palo Alto, CA 94304-1050
rshulman@wsgr.com
jholloway@wsgr.com

M. Craig Tyler, Esq.
Brian D. Range, Esq.
Wilson Sonsini Goodrich & Rosati
8911 Capital of Texas Highway North
Westech 360, Suite 3350
Austin, TX 78759
ctyler@wsgr.com
brange@wsgr.com

/s/ Philip A. Rovner
Philip A. Rovner (#3215)
Potter Anderson & Corroon LLP
Hercules Plaza, 6th Floor
P. O. Box 951
Wilmington, DE 19899
(302) 984-6000
provner@potteranderson.com

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EXHIBIT A

VITA
MILTIADIS K. HATALIS

I. PERSONAL

Year and place of birth:	1959, Thessaloniki, Greece
Marital status:	Married (3 children)
Citizenship:	USA

II. EDUCATION

Doctor of Philosophy (Ph.D.)	Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, PA USA	1987
Master of Science (M.S.)	Electrical and Computer Engineering, State University of New York at Buffalo, NY, USA	1984
Batchelor of Science (B.S.)	Physics Aristotle University of Thessaloniki, Greece	1982

III. EMPLOYMENT

Academia

1995-today	Professor	Lehigh University, Bethlehem, PA Department Electrical & Computer Engineering
1991-1995	Associate Professor	Lehigh University, Bethlehem, PA Department Electrical & Computer Engineering
1987-1991	Assistant Professor	Lehigh University, Bethlehem, PA Department Electrical & Computer Engineering
1984-1987	Research Assistant	Carnegie Mellon University; Pittsburgh, PA Department Electrical & Computer Engineering
1982-1984	Teaching Assistant	State University of New York at Buffalo, NY Department Electrical & Computer Engineering

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1993-today	Director	Display Research Laboratory Lehigh University
1988-1993	Associate Director	Microelectronics Research Laboratory Lehigh University

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Industry

1987-today	Consultant	IBM, Kodak, Litton, Corning, Spire, Sharp, eMagin, Sterling Diagnostics, Diamonex Dow Corning, Intevac, etc
1992	Visiting Scientist	XEROX Palo Alto Research Laboratory

IV. TEACHING RECORD

- Microelectronics Technology
- Fundamentals of Semiconductor Devices
- Semiconductor Materials and Device Characterization
- Thin Film Materials and Devices
- Introduction to VLSI Design

V. EDITOR

"Flat Panel Display Materials II"
Materials Research Society Symposium Proceedings vol. 424
Published by the Materials Research Society, 1997
"Proceedings of the Second International Workshop on Active Matrix Liquid Crystal Displays"
Published by the IEEE Society, 1996

VI. SUPERVISION OF STUDENTS

Ph.D. Dissertations:

1. F. Lin (1994) "Structural and Electrical Characteristics of Polycrystalline Semiconductors for Thin Film Transistor Applications"
2. A. Voutsas (1994) "Low Temperature Deposition of Polycrystalline Silicon for Active Matrix Liquid Crystal Applications"
3. K. Olasupo (1994) "Physics and Technology of Submicron Polysilicon Thin Film Transistors."
4. J. Kung (1994) "Effect of Gate Dielectric on Performance of Polysilicon Thin Film Transistors"
5. G. Sarcona (1995) "Effects of Silicides and Device Structure on the Characteristics and Circuit Performance of Polysilicon Thin Film Transistors for Active Matrix Liquid Crystal Display"
6. S. H. Lin (1995) "Physics, Technology and Characterization of Polysilicon Thin Film Transistors with Low Leakage Current Performance."
7. M. Stewart (1999) "Polysilicon Devices for Large Area Electronics Applications: Organic Light Emitting Diode Displays and X-Ray Sensors."
8. R. Howell (2000) "Advanced Metallization and Applications to Large Area Active Matrix Arrays and Polysilicon Thin Film Transistors"
9. F. Nkansah (2001) "Technology and Reliability of Sub-Micron 1T-Flash Electrically Erasable Programmable Read Only Memory (EEPROM)"
10. S. Karnik (2002) "Materials, Devices and Processes for Integrated Chemical Microsystems."
11. T. Afentakis (2004) "Active Matrix Technology for Flexible Displays and Biosensors"
12. S. Mukherjee (2006) "Integrated Microchemical Systems for Processing methanol Reformer Effluents for Portable Fuel Cell Applications." Co-Advised with Prof. M. Kothare
13. M. Troccoli (2006) "TFT Circuits for Display and Large Electronics on Metal Foils."
14. Ta-Ko Chuang (2007) "Active Matrix Organic Light Emitting Diode Displays on Flexible Metal Foil Substrates."

M.S. Thesis **10**
Post-Doctoral Supervision **3**

VII. ORGANIZATION OF SCIENTIFIC CONFERENCES

Chairman ***of the organization committee for the following workshops/conferences:***

International Workshop on Active Matrix Displays
It was sponsored by the Society of Information Display in co-operation with IEEE Electron Devices Society. It was held during the International Display Research Conference in Toronto, Canada, on September 20-23, 1997. There were 9 invited papers and 120 attendees.

Flat Panel Display Materials II
Meeting held during Spring1996 Meeting of the Materials Research Society. During the three day Symposium a total of 118 papers were presented. Prof. Hatalis was responsible for selecting the co-organizers, raising financial support for the event, prepare the technical program and edit the Symposium Proceedings.

Second International Workshop on Active Matrix Liquid Crystal Displays (AMLCDS ′95).
It was organized in co-operation with Society for Information Displays and the IEEE Electron Devices Society. It was held at Lehigh University on September 25-26, 1995. There were 11 invited and 25 contributed papers and 130 attendees.

First International Workshop on Active Matrix Liquid Crystal Displays
Workshop sponsored by the Society of Information Display in co-operation with IEEE Electron Devices Society. It was held during the International Display Research Conference in Monterey CA, on October 10-13, 1994. There were 10 invited and 22 contributed papers and 170 attendees.

Active Matrix Liquid Crystal Displays Symposium (AMLCDS ′93)
It was organized in co-operation with Society for Information Display and IEEE Electron Devices Society. It was held at Lehigh University, on October 21-22, 1993. Seven invited and 35 contributed papers were presented. Attendance was 160.

Member ***of the organization committee for the following workshops/conferences:***

Active Matrix Liquid Crystal Displays Technology and Applications
Sponsored by the International Society for Optical Engineering (SPIE).
USA, 1997

Sixth International Conference on Polycrystalline Semiconductors
Conference was held in FRANCE, 2000

Flat Panel Display Technology II
Sponsored by the International Society for Optical Engineering (SPIE).
USA, 2001

EURO-CVD Conference
Sponsored by the European Materials Research Society GREECE, 2001

International Workshop on Active Matrix Liquid Crystal Displays
Sponsored by the Japan Society of Applied Physics
JAPAN, 1999, 2000, 2001, 2002, 2003, 2004, 2005

VIII. RESEARCH RECORD

Ph.D. Dissertation:

"Low Temperature Crystallization of Amorphous LPCVD Silicon Films and Application to Bipolar and Thin Film Transistors"
Carnegie Mellon University, USA, 1987.

Book Chapters:

"Technology of Polysilicon Thin Film Transistors." A. T. Voutsas and M. K. Hatalis. Chapter 4 in the book "Thin Film Transistors" edited by C. Kagan and P. Andy. Published by Marcel Dekker, Inc. 2003.

"AMOLED Display Pixel Electronics." M. Troccoli, M. K. Hatalis, A. T. Voutsas, , Chapter 10, in the book "Organic Electroluminescence" edited by Z. Kafafi and H. Murata. Published by CRC Press & SPIE Press, 2005, p. 355.

Journal Papers

1. "High Performance Thin Film Transistors in Low Temperature Crystallized Amorphous Silicon Films" *IEEE Electron Device Letters*, vol. EDL-8, pp. 361-364, 1987. M. K. Hatalis and D. W. Greve
2. "Solid Phase Epitaxy of LPCVD Amorphous Silicon Films." *Journal of the Electrochemical Society*, vol. 134, pp. 2536-2540, 1987. M.K. Hatalis and D.W. Greve
3. "Large Grain Polycrystalline Silicon by Low Temperature Annealing of LPCVD Amorphous Silicon Films." *Journal of Applied Physics*, vol. 63, pp. 2260-2266, 1988. M.K. Hatalis and D.W. Greve
4. "Interfacial Oxide, Grain Size and Hydrogen Passivation Effects on Polysilicon Emitter Transistors", *IEEE Transactions on Electron Devices*, vol. ED-35, pp. 1334-1343, 1988. P.A. Potyraj, D.L. Chen, M.K. Hatalis, and D.W. Greve
5. "Minimum Detectable Solute Concentration by Atomic - Resolution TEM." *Acta Crystallographica A*, vol. A44, pp. 449-461, 1988. J.M. Howe, D.P. Basile, N. Prabhu, and M.K. Hatalis
6. "Low Temperature Polycrystalline Silicon Thin Film Transistors for Displays" *IEEE Transactions on Electron Devices*, vol. ED-35, pp. 1842-1845, 1988. B.C. Hseih, M.K. Hatalis and D.W. Greve
7. "Alternate Surface Cleaning Approaches for UHV/CVD Epitaxy of Si and GexSi1-x."*Journal of the Electrochemical Society*, vol. 138, pp. 3783-3789, 1991. M. Racanelli, D.W. Greve, M. K. Hatalis and L. J. van IJzendroorn
8. "Investigations on Quality of Polysilicon Film-Gate Dielectric Interface in Polysilicon Thin Film Transistors." *Thin Solid Films*, vol. 216, pp. 137-141, 1992. J.-H. Kung, M. K. Hatalis and J. Kanicki
9. "Flourine-Enhanced Oxidation of Polycrystalline Silicon and Application to Thin Film Transistor Fabrication" *Applied Physics Letters*, vol. 61, pp. 937-939, 1992. D. N. Kouvatsos, M. K. Hatalis and R. J. Jaccodine
10. "Structure of as-Deposited LPCVD Silicon Films at Low Deposition Temperatures and Pressures." *Journal of the Electrochemical Society*, vol. 139, pp. 2659-2665, 1992. A. T. Voutsas and M. K. Hatalis
11. "Surface Treatment Effect on the Grain Size and Surface Roughness of as Deposited LPCVD Silicon Films." *Journal of the Electrochemical Society*, vol.140, pp. 282-288, 1993. A. T. Voutsas and M. K. Hatalis

12. "Deposition and Crystallization of a-Si Low Pressure Chemically Vapor Deposited Films Obtained by Low-Temperature Pyrolysis of Disilane." *Journal of the Electrochemical Society*, vol. 140, pp. 871-877, 1993. A. T. Voutsas and M. K. Hatalis
13. "Crystallized Mixed-Phase Silicon Films for Thin Film Transistors on Glass Substrates." *Applied Physics Letters*, vol. 63, pp. 1546-1548, 1993. A.T. Voutsas and M.K. Hatalis
14. "Properties of the Cadmium Selenide Thin Films as a Function of Lateral Distance from Chromium Contacts", *Journal of the Electrochemical Society*, vol. 140, pp. 2994-2998, 1993. D. Waechter, M. R. Westcott, F. Lin, and M. K. Hatalis.
15. "Structural Characteristics of as-Deposited and Crystallized Mixed-Phase Silicon Films." *Journal of Electronic Materials*, vol. 23, pp. 319-330, 1994. A. T. Voutsas and M. K. Hatalis
16. "Experimental and Theoretical Study on the Crystallization of Chemically Vapor Deposited Mixed-Phase Silicon Films", *Journal of Applied Physics*, vol. 76, pp. 777-790, 1994. A. T. Voutsas and M. K. Hatalis
17. "Characterization of Cobalt Annealed on Silicon-Germanium Epilayers." *Thin Solid Films*, vol. 250, pp. 20-25, 1994. F. Lin, G. Sarcona, M. K. Hatalis, A. Cherhati, E. Austin and D. W. Greve
18. "Raman Spectroscopy of Amorphous and Microcrystalline Silicon Films Deposited by Low Pressure Chemical Vapor Deposition" *Journal of Applied Physics*, vol. 78, pp. 6999 - 7005, 1995. A. T. Voutsas, M. K. Hatalis, J. Boyce and A. Chiang
19. "High performance thin film transistors in large grain size polysilicon deposited by thermal decomposition of disilane,"*IEEE Transactions on Electron Devices*, vol. 43, pp. 1399 - 1406, 1996. D. N. Kouvatsos, A. T. Voutsas, and M. K. Hatalis
20. "Leakage current mechanism in submicron polysilicon thin film transistors"*IEEE Transactions on Electron Devices*, vol. 43, pp. 1218 - 1223, 1996. K. Olasupo and M. K. Hatalis
21. "The effect of drain offset on current-voltage characteristics in sub-micron polysilicon thin film transistors", *IEEE Transactions Electron Devices*, vol. 43, pp. 1306-1308, 1996. K. Olasupo, W. Yarbrough and M. K. Hatalis
22. "Single crystal silicon thin film transistors fabricated at low process temperatures on glass substrates" *Electronics Letters*, vol. 32, pp. 775 - 777, 1996. N. Kouvatsos, D. Tsoukalas, G. T. Sarcona, M. K. Hatalis and J. Stoemenos
23. "Polycrystalline silicon thin film transistors fabricated at reduced thermal budgets by utilizing fluorinated gate oxidation." *IEEE Transactions on Electron Devices*, vol. 43, pp. 1448 - 1453, 1996. D. N. Kouvatsos and M. K. Hatalis
24. "Nickel Silicides Grown on Amorphous Silicon and Silicon-Germanium Thin Films." *Electrochemical and Solid State Letters*, vol. 1, p. 233-234, 1998. G. Sarcona, S. K. Saha, and M. K. Hatalis
25. "Non-Erratic Behavior of Overerased Bits in Flash EEPROM" *Journal of Vacuum Science and Technology B*, vol. 16, p 3065-3068, 1998. F. Nkansah, E. Prinz, and M. K. Hatalis
26. "Thin Film Transistors in Low Temperature As-deposited and Reduced Crystallization-Time Polysilicon on 665 C Strain Point Glass Substrates." *Thin Solid Films*, vol. 338, pp. 281-285, 1999. M. K. Hatalis, D. N. Kouvatsos, J. H. Kung, A. T. Voutsas, and J. Kanicki
27. "Silicidation Reactions with Co – Ni Bilayers for Low Thermal Budget Microelectronic Applications." *Thin Solid Films*, vol. 347, pp. 278-283, 1999. S. K. Saha, R. S. Howell, and M. K. Hatalis

28. "Effect of Flash EEPROM Floating Gate Morphology on Electrical Behavior of Fast Programming Bits." *IEEE Transaction on Electron Devices*, vol. 46, pp. 1355-1362, 1999. F. Nkansah and M. K. Hatalis
29. "Polysilicon Thin Film Transistors using Self-Aligned Cobalt and Nickel Silicide Source and Drain contacts"*IEEE Electron Device Letters*, vol. 20, pp. 332-334, 1999. G. Sarcona, M. Stewart, and M. K. Hatalis
30. "Elimination of Hillock Formation in Al Interconnects Using Ni or Co" *Journal of Applied Physics*, vol. 86, pp. 625-633, 1999. S. K. Saha, R. S. Howell, and M. K. Hatalis
31. "Reaction Mechanisms in Al-ITO Ohmic Contact Metallization with Co and Ni Barrier Layers for Active Matrix Display Applications." *Journal of Electrochemical Society*, vol. 146, pp. 3134-3138, 1999. S. K. Saha, R. S. Howell, and M. K. Hatalis
32. "Polycrystalline Silicon Thin Film Transistors in Various Solid Phase Crystallized Films Deposited on Glass Substrates"*Journal of Electronic Materials*, vol. 28, pp. 19-25, 1999. D. N. Kouvatsos, A. T. Voutsas, and M. K. Hatalis
33. "Preparation and Stability of Low Temperature Cobalt and Nickel Silicides on Thin Polysilicon Films." *Journal of Vacuum Science and Technology A*, vol. 18, pp. 97-93, 2000. R. S. Howell, G. Sarcona, and M. K. Hatalis
34. "Poly-Si Thin Film Transistors on Steel Substrates" *IEEE Electron Device Letters*, vol. 21, pp. 70-72, 2000. R. S. Howell, M. Stewart, S. V. Karnik, S. K. Saha, and M. K. Hatalis
35. "High Performance Gated Lateral Polysilicon PIN Diodes", *Solid State Electronics*, vol. 44, pp.1613-1619, 2000. M. Stewart and M. K. Hatalis
36. "Characterization and Modeling of Fast Programming Bits in Flash EEPROM" *Solid State Electronics*, vol. 44, pp. 1887-1897, 2000. F. Nkansah, M. K. Hatalis and K. Olasupo
37. "Polysilicon TFT Technology for Active Matrix OLED Display", *IEEE Transaction on Electron Devices*, vol. 48, pp. 845-851, 2001. M. Stewart, R. S. Howell, L. Pires, and M. K. Hatalis
38. "Novel Cleaning Methodology for Steel Substrates in Microelectronic Fabrication." *Journal of Electrochemical Society*, vol. 149, pp. G143-G146, 2002. R. S. Howell and M. K. Hatalis
39. "Trade Off Between Polysilicon Film Quality and Thin Film Transistor Operational Amplifier DC Gain." Solid State Electronics, vol. 46/9, pp. 1421-1425, 2002. T. Afentakis and M. K. Hatalis.
40. "A Simple Analytical Model for the Dependence of the Propagation Delay of the Polycrystalline Silicon CMOS Inverter on Temperature" Solid State Electronics, vol. 46/12, pp. 2301-2306, 2002 T. Afentakis and M. K. Hatalis
41. "Palladium based Micro-Membrane for Water Gas Shift Reaction and Hydrogen Gas Separation." J. of Microelectromechanical Systems, vol. 12, pp.: 93- 100, 2003. S. V. Karnik, M. K. Hatalis, M. V. Kothare.
42. "Implementations of Rapid Thermal Processes in Polysilicon TFT Fabrication." Accepted for Publication by Elsevier for a Special Volume on Rapid Thermal Processing for Future Semiconductor Devices M. K. Hatalis and A. T. Voutsas
43. "Lateral Polysilicon p^+-p-n^+ and p^+-n-n^+ Diodes." *Solid State Electronics*, Vol. 47, pp. 653-659, 2003 S. V. Karnik and M. K. Hatalis
44. "Multiple Lateral Polysilicon Diodes as Temperature Sensors for Chemical Microreaction Systems," Japanese Journal of Applied Physics (JJAP), vol. 42, pp.1200-1205, 2003. S.V. Karnik and M. K. Hatalis
45. "Macroelectronics: Perspectives on Technology and Applications," Proceedings of IEEE, vol. 93, pp.1239-1256, 2005. R. H. Reuss, et.al. (M. Hatalis).

46. "Polysilicon TFT Circuits on Flexible Stainless Steel Foils," Solid State Electronics, vol. 50, pp 1080-1087, 2006. M. Troccoli, A. J. Roudbari, T. Chuang, M. Hatalis.
47. "Exciton dissociation by a static electric field followed by nanoscale charge transport in PPV polymer films," *Phys. Rev. B (Condensed Matter and Materials Physics),* vol. 73, p. 125202, 2006.
H. Najafov, I. Biaggio, Ta-Ko. Chuang, M. K. Hatalis.
48. "Design and fabrication of high-performance polycrystalline silicon thin-film transistor circuits on flexible steel foils" *IEEE Transactions on Electron Devices*, v 53, p 815-22, 2006. T. Afentakis, M. Hatalis, A. Voutsas and J. Hartzell.
49. "Water Gas Shift Reaction in a Glass Microreactor", *Catalysis Today*, vol. 120, p.107–120, 2007. S. Mukherjee, M. K. Hatalis, and M. V. Kothare.
50. "Top-emitting 230 dots/in. Active-Matrix Polymer Light-Emitting Diode Displays on Flexible Metal Foil Substrates," *Applied Physics Letters* 90, 151114 (2007).
T.-K. Chuang, M. Troccoli, P.-C Kuo, A. Jamshidi, M. K. Hatalis; I. Biaggio; A. T. Voutsas,
51. "Polysilicon TFT technology on Flexible Metal Foils for AM-PLED displays," Invited paper: *Journal of Society for Information Displays*, 15, 455 (2007). T.-K. Chuang, M. Troccoli, M. K. Hatalis, and A. T. Voutsas,
52. "Process Technology for High-Resolution AM-PLED Displays on Flexible Metal Foil Substrates," *Electrochemical and Solid-State Letters*, 10, J92 (2007).
T.-K. Chuang, M. Troccoli, P.-C Kuo, A. Jamshidi, M. K. Hatalis, A. T. Voutsas, and T. Afentakis,

Refereed Conference Papers

1. "Solid Phase Epitaxy of LPCVD Silicon Films and Their Use as Diffusion Sources." *The Electrochemical Society Extended Abstracts*, Vol. 86-1, Spring 1986. M. K. Hatalis and D. W. Greve
2. "TEM Studies of the Amorphous / Crystalline Transition in Silicon and Applications to Electronic Devices." *Institute Physics Conference Series*, vol. 87, pp. 479-484, 1987 D.W. Greve and M. K. Hatalis
3. "Crystallization of Amorphous LPCVD Silicon Films and Application to Bipolar and Thin Film Transistors." *Materials Research Society Symposium Proceedings*, vol. 106, pp. 335-340, 1987 M. K. Hatalis and D. W. Greve
4. "Thin Film Transistors in Low Temperature Crystallized Amorphous Silicon Films." *The Electrochemical Society Extended Abstracts*, Vol. 87-1, Spring 1987. M. K. Hatalis and D. W. Greve
5. "Minimum Detectable Solute Concentration and Accuracy of Compositional Analysis in Atomic-Resolution Microscopy." *Proceedings Microbeam Analysis Society*, 22nd Annual Mtg., Hawaii, Summer 1987 J. M. Howe, D. P. Basile, N. Prabhu and M. K. Hatalis
6. "Electrical Characteristics of Polysilicon Thin Film Transistors at Low Temperatures." *Proceedings International Topical Conference on Hydrogenated Amorphous Silicon Devices and Technology*1988 M. K. Hatalis and N. Stylianou
7. "Effect of Annealing on Grain Size of Undoped and Indium Doped CdSe Thin Films."*The Electrochemical Society Extended Abstracts*, Vol. 89-1, Spring 1989 M. K. Hatalis and M. R. Westcott

8. "Structural and Electrical Characterization of CdSe Thin Films." *Materials Research Society Symposium Proceedings,* vol. 164, pp. 87-92, 1990 M. K. Hatalis, F. Lin and M. Westcott
9. "Effect of Gate Dielectric on Performance of Polysilicon Thin Film Transistors." *Materials Research Society Symposium Proceedings,* vol. 182, pp. 357-362, 1990 M. K. Hatalis, J. H. Kung, J. Kanicki and A. Bright
10. "Hydrogenation of Polycrystalline Silicon Thin Film Transistors." *The Electrochemical Society Extended Abstracts,* Vol. 91-1, Abstract 410, pp. 629-630, spring 1991 M. K. Hatalis, J. H. Kung and J. Kanicki
11. "Effect of Temperature and Pressure on the Structure of LPCVD Polysilicon Films." *The Electrochemical Society Extended Abstracts,* Vol. 91-1, Abstract 416, pp. 639-640, Spring 1991 A. Voutsas and M. K. Hatalis
12. "Nucleation and Crystallization of Amorphous Silicon-Aluminum Thin Films" *Materials Research Society Symposium Proceedings,* vol. 230, pp. 195-200, 1992 F. Lin, M. K. Hatalis, S. Girginoudi, D. Girginoudi, N. Georgoulas and A. Thanailakis.
13. "A Simple Polysilicon TFT Structure for Achieving High On/Off Current Ratio Independent upon Gate Bias", *International Conference on Solid State Devices and Materials,* Japan, Fall 1992. J. Kanicki and M. K. Hatalis.
14. "Thin Silicon Dioxide Films Grown at Very Low Oxygen Partial Pressure in Oxygen Diluted by Helium", *The Electrochemical Society Extended Abstracts,* Vol. 92-2, Fall 1992 D. N. Kouvatsos and M. K. Hatalis
15. "Polysilicon TFTs with various 800°C Thermally Grown Gate Oxides" *The Electrochemical Society Extended Abstracts,* Vol. 92-2, Fall 1992 J.-H. Kung, D. N. Kouvatsos and M. K. Hatalis
16. "Properties of cadmium selenide thin films as a function of lateral distance from chromium contacts (TFT)", *The Electrochemical Society Proceedings of the 1st Symposium on Thin Film Transistor Technologies"*, p. 235, 1992 D. Waechter, F. Lin, M. K. Hatalis
17. "Hydrogenation effects on polysilicon thin-film transistor structures" 50th Annual Device Research Conference, IEEE Transactions on Electron Devices, vol. 39, p. 2665, 1992. M. K. Hatalis, J. H. Kung, and J. Kanicki.
18. "Deposition and Characterization of Crystallized LPCVD Si-films Obtained by Low Temperature Pyrolisis of Disilane", *The Electrochemical Society Extended Abstracts,* Vol. 92-1, Spring 1992. A. T. Voutsas and M. K. Hatalis
19. "Crystallization of Tin-Implanted Amorphous Silicon Thin Films", *Materials Research Society Symposium Proceedings,* vol. 279, pp. 553-558, 1993 F. Lin and M. K. Hatalis
20. "A New Quantitative Roughness Measurement and its Application in the Polysilicon/Silicon Dioxide Interface." *Materials Research Society Symposium Proceedings,* vol. 280, pp. 285-288, 1993 S. Lin and M. K. Hatalis
21. "Electrical and Structural Properties of Cobalt Annealed on Silicon-Germanium Epilayers", *Materials Research Society Symposium Proceedings,* vol. 281, pp. 647-652, 1993 G. Sarcona, F. Lin, M. K. Hatalis, A. F. Cherhati, E. Austin, and D. W. Greve
22. "Performance of Polycrystalline Silicon Thin Film Transistors with Double Layer Gate Dielectric", *Materials Research Society Symposium Proceedings,* vol. 284, pp. 431-436, 1993 J. H. Kung, M. K. Hatalis and J. Kanicki

23. "Fluorinated Silicon Dioxide Films as Gate Dielectrics of Polysilicon Thin Film Transistors", *Materials Research Society Symposium Proceedings"*, vol. 284, pp. 437-442, 1993 D. N. Kouvatsos, J. H. Kung, M. K. Hatalis and J. Kanicki
24. "A Novel Low-Temperature LPCVD Process for Deposition of Polysilicon Films on Glass Substrates", *The Electrochemical Society Proceedings, 12th International Conference on CVD*, Honolulu, Hawaii, May 1993 A. T. Voutsas and M. K. Hatalis
25. "Low Temperature Polysilicon Thin Film Transistors on Corning Code 1734 and 1735 Glass Substrates." *Society for Information Displays International Symposium Digest*, vol. 24, 1993 M. K. Hatalis, D. N. Kouvatsos, J.-H. Kung, A. T. Voutsas, F. P. Fehlner, and J. Kanicki
26. "Amorphous Silicon and Silicon-Germanium Thin-Film Transistors Formed by Ion Implantation", *Materials Research Society Symposium Proceedings"*, vol. 297, pp. 907-912, 1993 G. T. Sarcona, M. K. Hatalis, and A. Catalano
27. "Nucleation and Grain Growth in Silicon Films Deposited by Thermal Decomposition of Disilane" *Materials Science Forum"*, vol. 126-128, pp. 431-434, 1993 Presented at the 6th International Conference on Intergranular and Interface Boundaries in Materials A. T. Voutsas and M. K. Hatalis
28. "Rapid Thermal Crystallization of LPCVD Amorphous Silicon Films", *Materials Research Society Symposium Proceedings*, vol. 345, pp. 93-98, 1994 A. T. Voutsas, M. K. Hatalis, K. R. Olasupo, A. K. Nanda and D. Alugbin
29. "Characteristics of Sub-Micron Polysilicon Thin film Transistors" *Materials Research Society Symposium Proceedings*, vol. 345, pp. 129-134, 1994. K. Olasupo, M. K. Hatalis
30. "Polysilicon TFT Technology for High Functionality Active Matrix Liquid Crystal Displays", *Proceedings of the 1994 IEEE Princeton/Central Jersey Sarnoff Symposium*, INVITED PAPER M. K. Hatalis.
31. "Effect of Grain Size and Process Temperature on Distribution of Polysilicon TFT's Electrical Characteristics", M. K. Hatalis, D. Kouvatsos, S.-H. Lin, and A. T. Voutsas Conference Record of*14th Annual International Display Research Conference*, pp. 150-153, 1994 published by Society for Information Displays
32. "Materials and Device Aspects of Polysilicon TFT-LCD Technology." *Proceedings of the Second International Display Workshops*, vol. 2, pp. 3-6, 1995, (Japan) INVITED PAPER M. K. Hatalis.
33. "Polysilicon TFT Active Layer Fabrication Processes." M. K. Hatalis. INVITED PAPER Presented at the *"International Active Matrix Workshop"* held with the Euro Display '96: "The 16th International Display Research Conference." (October 1996). Paper published in the Proceedings of 1996 International Active Matrix Workshop, pp. 21-24, 1996
34. "Low Temperature Silicides for Polysilicon Thin Film Transistor Applications" *Materials Research Society Symposium Proceedings*, vol. 402, pp.191-196, 1996. G. Sarcona and M. K. Hatalis
35. "Polysilicon Thin Film Transistors with Cobalt and Nickel Silicide Source and Drain Contacts" *Materials Research Society Symposium Proceedings*, vol. 424. pp. 159-164, 1997 G. Sarcona and M. K. Hatalis
36. "Helical Resonator Plasma Oxidation of Amorphous Silicon for Flat Panel Display", *Materials Research Society Symposium Proceedings*, vol. 424. pp. 165-170, 1997 S. Kaluri, R. Howell, M. K. Hatalis and D. W. Hess
37. "Polysilicon TFT Active Matrix Organic EL Displays" *SPIE Proceedings Series*, vol. 3057, pp.277-286, 1997 M. K. Hatalis, M. Stewart, C. Tang, and J. Burtis

38. "Silicides for Polysilicon TFT-LCD applications", *SPIE Proceedings Series*, vol. 3014, pp.141-146, 1997 R. S. Howell, M. J. Stewart, G. Sarcona, and M. K. Hatalis
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IX. RESEARCH FUNDING

Total number of research programs: 26
Total budget: $ 12,584,718

A. Research Programs as Principal Investigator

Total budget as Principal Investigator: $ 9,704,718

1. Title: "Silicon Alloy Thin Films for Solar Cells and Displays"
   Agent: State of Pennsylvania / Solarex Corp.
   Amount: **$45,000** Period: 9/88-8/89

2. Title: "Thin Film Transistor Studies"
   Agent: IBM
   Amount: **$150,750** Period: 9/89-8/91

3. Title: "Low temperature Polycrystalline Films for Display Applications"
   Agent: Litton Systems Canada Inc.
   Amount: **$58,000** Period: 1989, unrestricted duration

4. Title: "Polysilicon TFTs for Advanced Flat Panel Displays"
   Agent: Advanced Research Program Agency
   Amount: **$126,500** Period: 10/90-9/91

5. Title: "Development of Electronic Grade CVD Diamond"
   Agent: State of Pennsylvania / Diamonex Inc.
   Amount: **$125,000** Period: 9/91-8/93

6. Title: "High Performance Polysilicon TFTs for Advanced Flat Panel Displays"
   Agent: Advanced Research Program Agency
   Amount: **$260,000** Period: 9/91-8/92

7. Title: "Advanced Materials and Devices for High Definition TFT-LCD Displays"
   Agent: Advanced Research Program Agency
   Amount: **$1,170,000** Period: 9/92-5/96

8. Title: AASERT Award I "Advanced Materials and Devices for High Definition TFT-LCD Displays"
   Agent: Advanced Research Program Agency
   Amount: **$216,600** Period: 9/94-8/97

9. Title: AASERT Award II "Advanced Materials and Devices for High Definition TFT-LCD Displays"
   Agent: Advanced Research Program Agency
   Amount: **$200,000** Period: 9/95-8/98

10. Title: "Low Temperature Polysilicon TFTs in Advanced Display Technologies"
    Agent: Advanced Research Program Agency
    Amount: **$1,498,000** Period: 6/96-8/99

11. Title: "Acquisition of Advanced Equipment for Rapid Thermal and High Density Plasma Processing for Integrated Circuits and Flat Panel Displays"
Agent: National Science Foundation
Amount: **$130,000** Period: 9/96-8/99

12. Title: "Polysilicon pin Diode Based Direct x-Ray Sensor Array for Application in Fluoroscopy and Radiography"
Agent: Sterling Diagnostic Inc.
Amount: **$150,000** Period: 9/97-12/98

13. Title: "Flexible AMOLED Displays on Metal Foils."
Agent: Army Research Laboratory / Lehigh cooperative program
Amount: **$1,190,000** Period: 9/03 – 4/05

14. Title: "High Performance Macroelectronics Systems for Antenna Applications"
Agent: DARPA, subcontract to Lehigh from Northrop Grumman
Amount: **$1,078,024** Period: 6/04-12/07

15. Title: "Polysilicon Thin Film Devices for Sensor Applications"
Agent: Ben Franklin Technology Partners of State of PA
Amount: **$300,000** Period: 7/05 – 6/07

16. Title: "Flexible VGA AMOLED & AMPLED Displays on Metal Foils"
Agent: Army Research Laboratory / Lehigh cooperative program
Amount: **$2,767,768** Period: 4/05 – 5/08

17. Title: "Array Electronics for Multichannel Carbon Nanotube Gas Sensors"
Agent: NASA / Lehigh cooperative program
Amount: **$114,076** Period: 6/06 – 6/08

18. Title: "Comparison of Different Metal Foils for Flexible Displays"
Agent: United States Display Consortium
Amount: **$125,000** Period: 12/07 –11/08

B. Research Programs as Co-Principal Investigator: (total $ 2,880,000)

1. Title: "Physical Electronics of Multi-Dielectric Microstructures."
Agent: National Science Foundation
Amount: **$55,000** Period: 9/89-5/90 P.I.: M. White

2. Title: "Plasma Oxidation/Anodization of Si films for Photovoltaic and Flat Panel Display Applications"
Agent: National Science Foundation
Amount: **$237,000** Period: 9/92-8/95 P.I.: D. W. Hess,

3. Title: "Acquisition of an Automated Digital Transmission Electron Microscope"
Agent: National Science Foundation
Amount: **$709,300** Period: 6/96-8/99 P.I.: D. Smith

4. Title: "An Integrated Chemical Reforming Microplant for Fuel Cell Applications"
   Agent: National Science Foundation
   Amount: **$533,000** Period: 11/99 – 10/02 P.I.: M. Kothare

5. Title: "Large Area Biosensing electronics"
   Agent: National Science Foundation
   Amount: **$835,300** Period: 8/00 – 7/03 P.I.: D. W. Greve

6. Title: "Smart Microchemical Plant-on-Chip for High Performance Microscale Portable Power"
   Agent: Pittsburgh Digital Greenhouse
   Amount: **$150,400** Period: 9/01 – 8/02 P.I.: M. Kothare

7. Title: "Acquisition of an Advanced Electron Lithography System"
   Agent: National Science Foundation
   Amount: **$360,000** Period: 9/01 – 8/04 P.I.: M. White

8. Title: "Acquisition of an Advanced Electron Lithography System"
   Agent: National Science Foundation
   Amount: **$360,000** Period: 9/01 – 8/04 P.I.: M. White

EXHIBIT B

United States Patent [19]

Shimbo

[11] **Patent Number: 4,624,737**

[45] **Date of Patent: Nov. 25, 1986**

[54] **PROCESS FOR PRODUCING THIN-FILM TRANSISTOR**

[75] Inventor: **Masafumi Shimbo**, Tokyo, Japan

[73] Assignee: **Seiko Instruments & Electronics Ltd.**, Tokyo, Japan

[21] Appl. No.: **743,092**

[22] Filed: **Jun. 10, 1985**

[30] **Foreign Application Priority Data**

Aug. 21, 1984 [JP] Japan 59-173848

[51] **Int. Cl.**[4] **H01L 21/306**; B44C 1/22; C03C 15/00; C23F 1/02

[52] **U.S. Cl.** ..... **156/643**; 29/576 R; 29/578; 29/591; 156/652; 156/653; 156/656; 156/657; 156/659.1; 156/662; 156/667; 357/4; 357/23.1; 427/88; 427/93; 427/94

[58] **Field of Search** ..... 156/643, 646, 652, 653, 156/655, 656, 657, 659.1, 661.1, 662, 667, 668; 204/192 E, 192 EC; 427/38, 39, 88, 89, 90, 93, 94, 95; 430/313, 317, 318; 29/571, 576 R, 578, 591; 357/4, 23.1, 23.7, 65, 71

[56] **References Cited**

U.S. PATENT DOCUMENTS

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4,426,407	1/1984	Morin et al.	156/656 X

Primary Examiner—William A. Powell

Attorney, Agent, or Firm—Robert E. Burns; Emmanuel J. Lobato; Bruce L. Adams

[57] **ABSTRACT**

A gate insulating film, a high-resistivity semiconductor film, a low-resistivity semiconductor film and if necessary a conducting film are successively deposited in lamination without exposing them to any oxidizing atmosphere including atmospheric air, and then the source and drain electrodes are selectively formed.

4 Claims, 13 Drawing Figures

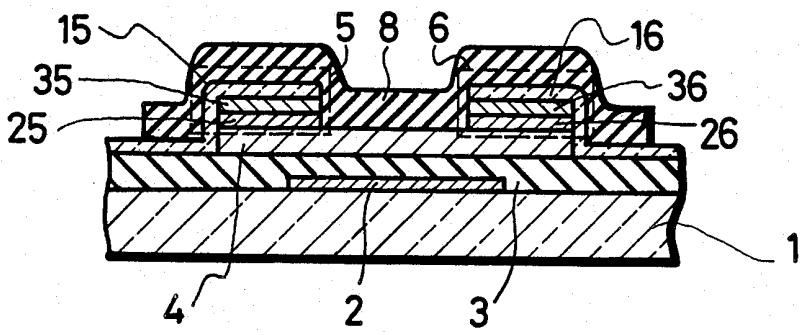


FIG. 1a PRIOR ART

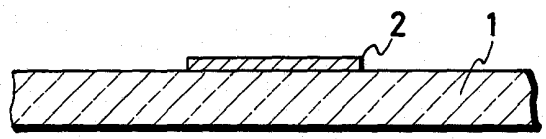


FIG. 1b PRIOR ART

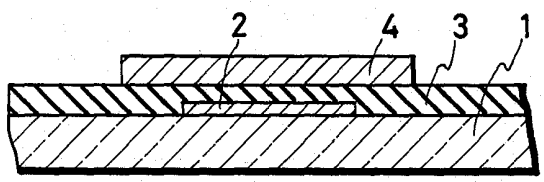


FIG. 1c PRIOR ART

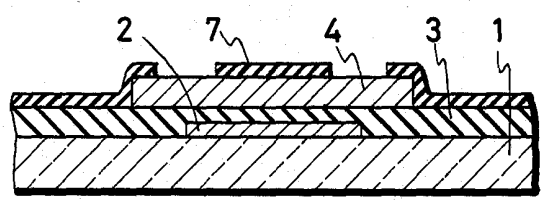


FIG. 1d PRIOR ART

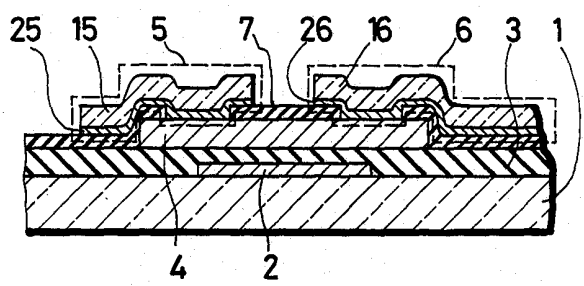


FIG. 2a

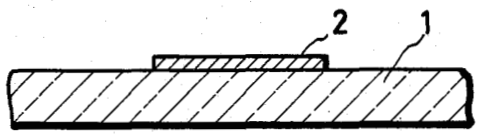


FIG. 2b

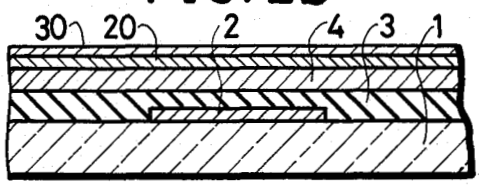


FIG. 2c

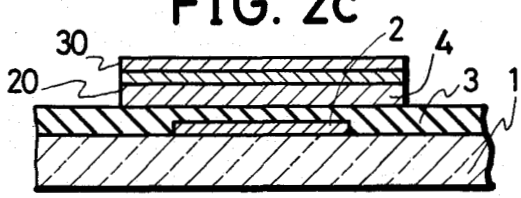


FIG. 2d

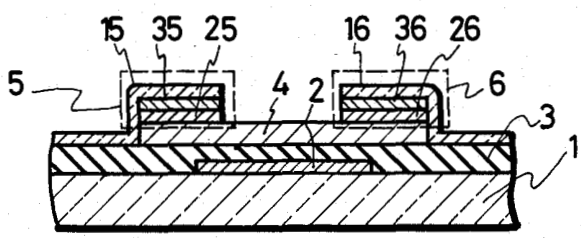


FIG. 2e

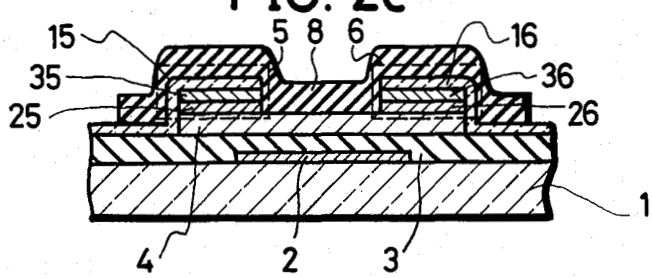


FIG. 3a

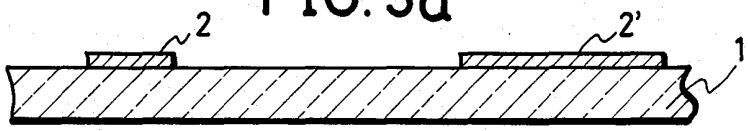


FIG. 3b

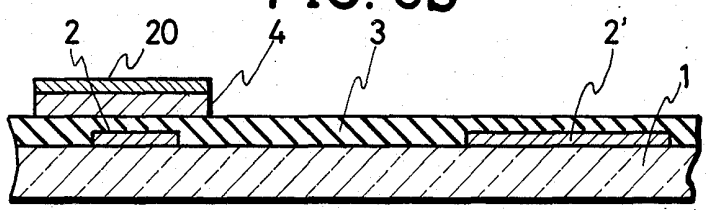


FIG. 3c

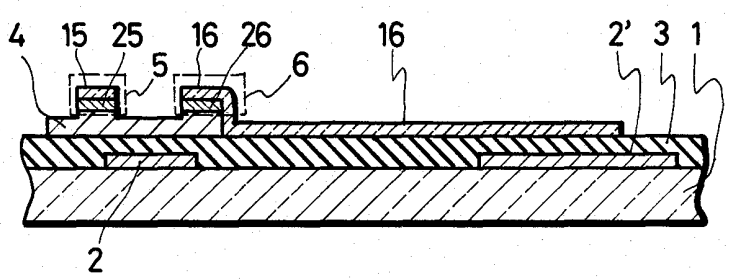
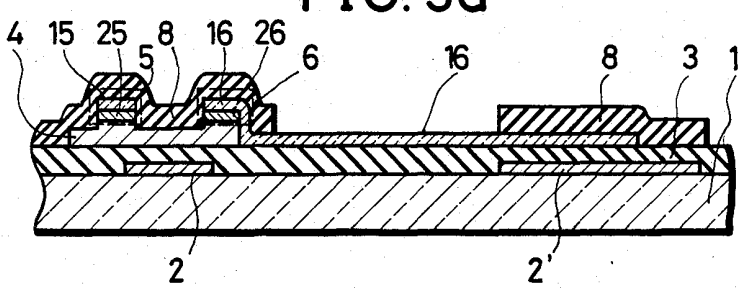


FIG. 3d



PROCESS FOR PRODUCING THIN-FILM TRANSISTOR

BACKGROUND OF THE INVENTION

This invention relates to a process for producing a thin-film transistor with improved performance.

Thin-film transistors (TFT) using semiconductor films of amorphous silicon (a-Si) or polycrystalline silicon (P-Si) are being applied to liquid crystal displays and like devices. Such thin-film transistors are diversified in structure. FIGS. **1***a* to **1***d* illustrate a conventional process for producing a thin-film transistor of a planar structure using amorphous silicon film. Shown in FIG. **1***a* in a sectional view is the initial step for selectively forming a gate electrode **2** on an insulating substrate **1** such as a glass substrate. Then, as shown in FIG. **1***b*, a gate insulating film **3** (such as silicon nitride film) and an amorphous silicon film **4** are continuously deposited, and said amorphous silicon film **4** is selectively etched. Then a field insulating film **7** (such as SiOx film) is deposited and windows for contact with source and drain regions are formed as shown in FIG. **1***c*. Although not shown, a gate contact window is also formed simultaneously. Thereafter, as illustrated in FIG. **1***d*, for instance n^+ amorphous silicon films **25**, **26** and metal (such as Al) films **15**, **16** are deposited and selectively etched to form drain and source electrodes **5**, **6**, thereby completing a thin-film transistor unit. If necessary, a surface passivation film and/or light-shielding film are further formed thereon.

In the conventional process shown in FIGS. **1***a* to **1***d*, since the masking step precedes the deposition of n^+ amorphous films **25**, **26**, natural oxide is produced on the exposed surface of amorphous silicon film **4**. Although such natural oxide can be removed by an aqueous solution of hydrofluoric acid (HF) or a similar substance, the possibility is still great that oxygen and its compounds as well as other impurities can collect on the laminate surface as it is exposed to the atmosphere. This would give rise to electrical resistance between the source and drain and between channels in the thin-film transistor thus obtained, making such transistor unable to exhibit its desired characteristics. A similar phenomenon would also occur at the interface of n^+ amorphous silicon films **25**, **26** and metal films **15**, **16**.

As described above, according to the conventional process, resistance would be generated between the source and drain and between channels and it was thus impossible to obtain the proper current flow and frequency characteristics. It was also a disadvantage of such conventional process that it was necessary to repeat the masking step as many as 5 to 6 times.

SUMMARY OF THE INVENTION

It is an object of present invention to provide a simplified process for producing a thin-film transistor with an improved contact arrangement.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1***a* to **1***d* are sectional views showing the sequential steps in a conventional thin-film transistor production process.

FIGS. **2***a* to **2***e* are sectional views illustrating stepwise a process for producing a thin-film transistor according to the present invention.

FIGS. **3***a* to **3***d* are sectional views illustrating the sequential steps for producing a thin-film transistor according to the process of this invention as it was applied to a substrate for liquid crystal display.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention will be described in detail below with reference to the accompanying drawings.

FIGS. **2***a* to **2***e* are sectional views illustrating a process for producing a thin-film transistor using amorphous silicon according to this invention. FIG. **2***a* shows in a sectional view the initial step for selectively forming a gate electrode **2** on an insulating substrate **1** such as glass, quartz, ceramic, insulator-coated silicon or metal. Metals such as Cr, Mo, W, Al, Ta, etc., and their silicides, impurity-doped polysilicon and other like materials can be used as said gate electrode **2**.

In the next step illustrated in FIG. **2***b* in a sectional view, a gate insulating film **3**, a high-resistivity film **4**, a low-resistivity a-Si:H (usually hydrogenated amorphous silicon) film **20** and a conducting film **30** made of a metal or other material are successively formed on said gate electrode **2** and substrate **1** without exposing them to an oxidizing atmosphere. Such successive deposition can be accomplished, for instance, by forming a silicon nitride (SiNx) film as gate insulating film **3** from a mixed gas of SiH_4 and NH_3, forming a high-resistivity a-Si:H film **4** by using SiH_4 and forming a n^+ a-Si:H film **20** from a mixed gas of PH_3 and SiH_4 in the same evacuated chamber in a plasma CVD apparatus. It is also possible to form said films successively in the respective chambers by using a plasma CVD apparatus having in-line chambers. Further, when a sputtering or metalizing chamber is additionally provided, conducting film **30** can be also deposited continuously without exposure to the atmosphere. Beside SiNx, a film of SiOx or a multi-layer film made of such materials can be used as said gate insulating film **3**. In place of said high-resistivity amorphous silicon film **4**, there can be used a film of amorphous silicon-fluorine alloy (a-Si:F) or amorphous silicon-hydrogen-fluorine alloy (a-Si:H:F) using, for instance, SiF_4, or a microcrystalline amorphous silicon film. Such alloys can be also used for said low-resistivity amorphous silicon film **20**, and such film may contain other impurites beside phosphorous impurities. As said conducting film **30**, it is desirable to use a stable conducting film such as a transparent conducting film made of a refractory metal such as Cr, W, Mo, Ta, etc., and silicides thereof, or indium-tin-oxide (ITO), SnO_2 and the like. Use of a transparent conducting film has the advantage that the process is simplified when the thin-film transistor of this invention is applied to an active matrix liquid crystal display.

FIG. **2***c* illustrates the step in which said conducting film **30**, low-resistivity amorphous silicon film **20** and high-resistivity amorphous silicon film **4** are left as an island region by etching in a single masking step. Known etching techniques such as wet etching, plasma etching, reactive ion etching, ion etching, etc., can be used for this step. Then, as illustrated in FIG. **2***d* in a sectional view, drain and source electrode members **15**, **16** are selectively provided, and conducting film **30** and low-resistivity amorphous silicon film **20** shown in FIG. **2***c* are selectively removed with said electrode members **15**, **16** serving at least as a part of the mask to form drain electrode **5** and source electrode **6**. In this step, it is desirable to clean the surface of conducting film **30** by proper etching means such as sputter etching or ion

etching before forming said drain and source electrode members **15**, **16**. In this case, the channel areas of the thin-film transistor are safe from damage by cleaning as they are covered with conducting film **30**. The same materials as used for conducting film **30** and other materials such as Al can be used for said drain and source electrode members **15**, **16**. When selectively etching low-resistivity amorphous silicon film **20**, no problem arises even if it is overetched to the extent that etching reaches the high-resistivity amorphous silicon film **4**.

In the final step illustrated in FIG. *2e*, a surface passivation film **8** is deposited, and the drain and source electrodes **15**, **16** and gate electrode **2** are partly exposed (not shown). A CVD film of SiOx, SiNx, etc., a resist or a coating of polyimide resin can be used as said surface passivation film **8**. If light shielding is required, a multilayer film composed of said insulating film and a metal or high-resistivity semiconductor film can be used as said surface passivation film **8**. When amorphous silicon-germanium alloy ($a\text{-}Si_{1-x}Ge_x$) is used as light-shielding film, surface passivation may not be necessary.

FIGS. *3a* to *3d* show sectionally a unit picture cell in an application of the present invention to the manufacture of a TFT substrate for liquid crystal display. FIG. *3a* illustrates a step in which gate electrode **2** extending along one line and gate electrodes **2'** on another line are formed on a transparent insulating substrate **1** such as glass substrate. Then, as illustrated in FIG. *3b*, gate insulating film **3**, high-resistivity amorphous silicon film **4** and low-resistivity amorphous silicon film **20** are deposited successively without exposure to an oxidizing atmosphere, and said low-resistivity amorphous silicon film **20** and high-resistivity amorphous silicon film **4** are left as an island region in the area where a thin-film transistor is to be formed.

In the next step illustrated in FIG. *3c*, a transparent conducting film such as ITO film is deposited; then, drain electrode **15** and source electrode **16** which doubles as a picture cell electrode are selectively formed and the exposed portion of low-resistivity amorphous silicon film **20** is removed. In this example, a charge-holding capacitor is formed by said picture cell electrode (source electrode) **16**, gate electrode **2'** and gate insulating film **3**. In the final step shown sectionally in FIG. *3d*, surface passivation film **8** concurrently serving as a light-shielding film is deposited and then selectively etched to expose picture cell electrode, drain electrode **15** and a part of gate electrodes **2**, **2'** (not shown). In this example, no conducting film is formed on low-resistivity amorphous silicon film **20**, but a conducting film such as ITO film may be formed on said low-resistivity film **20** as in the example shown in FIG. **2**.

As described above, according to the present invention, no oxides, etc., are formed at the interface of high-resistivity amorphous silicon film **4** and low-resistivity amorphous silicon film **20**, so that a good junction can be formed. The same is true with the interface of low-resistivity amorphous silicon film **20** and conducting film **30**. Further, since the interfaces of low-resistivity amorphous silicon film **20** or conducting film **30** and drain and source electrodes **15**, **16** can be cleaned without damaging the high-resistivity amorphous silicon film, a good contact can be obtained without sacrificing the inherent properties of thin-film transistor.

According to the present invention, as explained above, a thin-film transistor having good contact characteristics can be formed with only four masking operations. The present invention is especially effective for the production of thin-film transistors requiring a low temperature process such as thin-film transistors using amorphous silicon. It is thus possible with the present invention to obtain a thin-film transistor with small channel series resistance which improves driving performance and frequency characteristics.

While the present invention has been principally described regarding an embodiment thereof as applied to the production of a thin-film transistor using amorphous silicon by utilizing plasma CVD, the invention can as well be applied to the manufacture of thin-film transistors using semiconductor films by utilizing the photo CVD or molecular beam and/or the ion beam deposition method, thin-film transistors using polysilicon, and thin-film transistors using semiconductor films of other materials than silicon; consequently, the present invention is of great industrial significance.

I claim:

1. A process for producing a thin-film transistor comprising a first step for forming a gate electrode on an insulating substrate, a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere, a third step in which said high-resistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode, a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other, a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask, a sixth step for depositing a surface passivation film, and a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.

2. A process for producing a thin-film transistor according to claim **1**, wherein in said second step said conducting film is composed of at least two layers consisting of a low-resistivity semiconductor film and thereon a refractory metal film or transparent conducting film, and both of said films are continuously deposited without being exposed to the oxidizing atmosphere.

3. A process for producing a thin-film transistor according to claim **1** , wherein in said sixth step a light-shielding film is formed at a part of said surface passivation film.

4. A process for producing a thin-film transistor according to claim **2** , wherein in said sixth step a light-shielding film is formed at a part of said surface passivation film.

* * * * *

EXHIBIT C

US005825449A

United States Patent [19]

Shin

[11] **Patent Number: 5,825,449**

[45] **Date of Patent: Oct. 20, 1998**

[54] **LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME**

[75] Inventor: **Woo Sup Shin**, Kyungsangbuk-do, Rep. of Korea

[73] Assignee: **LG Electronics, Inc.**, Seoul, Rep. of Korea

[21] Appl. No.: **781,188**

[22] Filed: **Jan. 10, 1997**

Related U.S. Application Data

[62] Division of Ser. No. 616,291, Mar. 15, 1996.

[30] **Foreign Application Priority Data**

Aug. 19, 1995 [KR] Rep. of Korea 25538/1995

[51] **Int. Cl.**[6] **G02F 1/136**; G02F 1/1343; G02F 1/1345

[52] **U.S. Cl.** **349/148**; 349/149; 349/43

[58] **Field of Search** 349/149, 148, 349/43, 139, 152, 147

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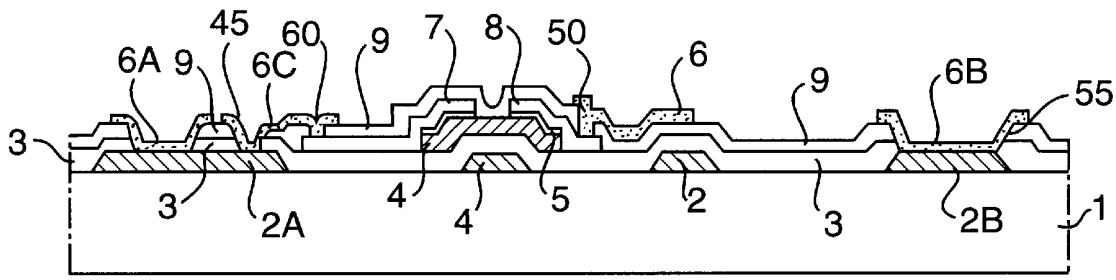
Primary Examiner—William L. Sikes
Assistant Examiner—Tiep H. Nguyen
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.

[57] **ABSTRACT**

A method for fabricating a liquid crystal display is disclosed whereby a source and gate are exposed after the step of forming a passivation layer. As a result, the number of processing steps is reduced and yield is improved.

11 Claims, 5 Drawing Sheets



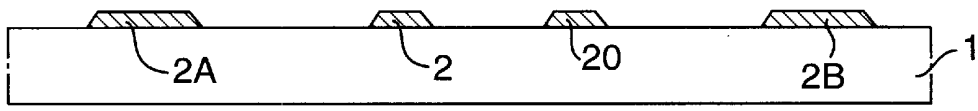


FIG. 1a
PRIOR ART

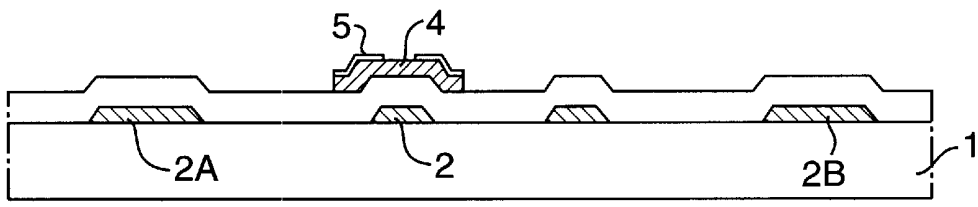


FIG. 1b
PRIOR ART

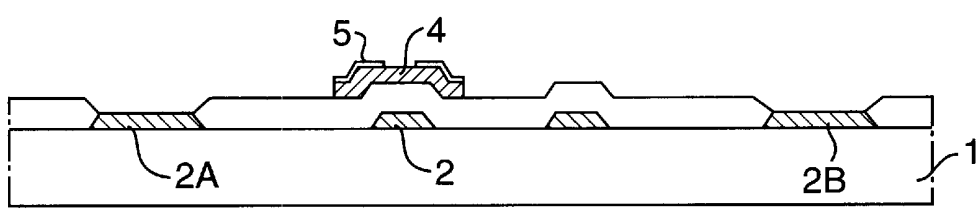


FIG. 1c
PRIOR ART

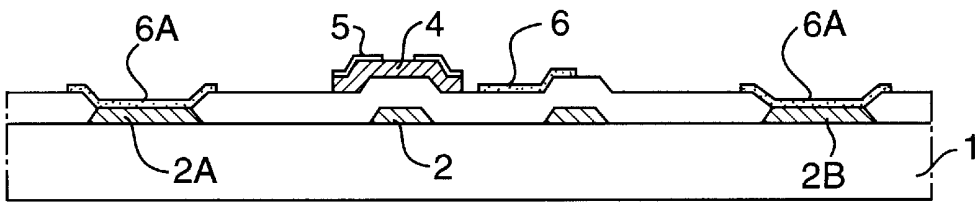


FIG. 1d
PRIOR ART

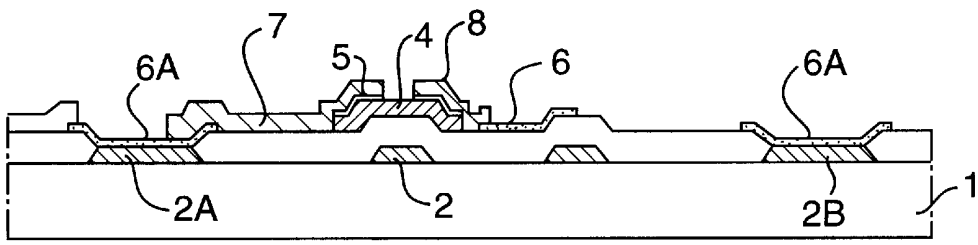


FIG. 1e
PRIOR ART

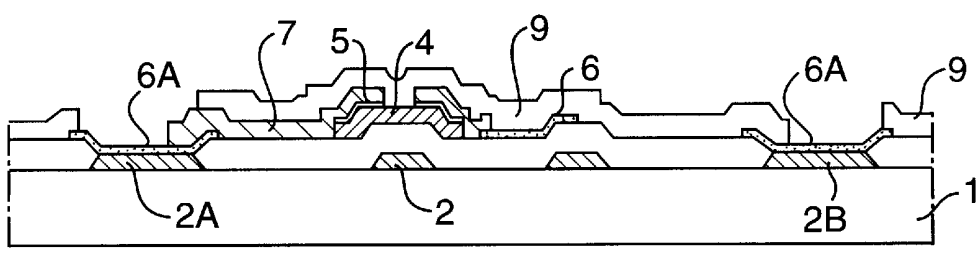


FIG. 1f
PRIOR ART

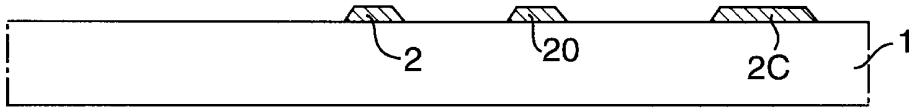


FIG. 2a

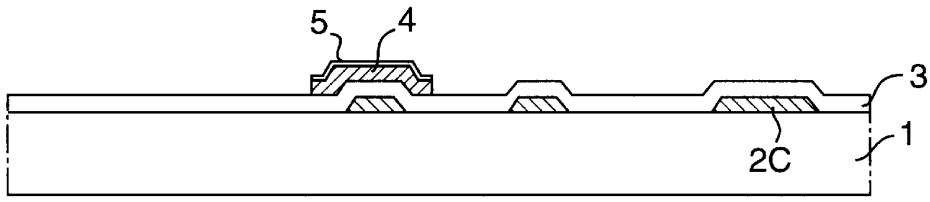


FIG. 2b

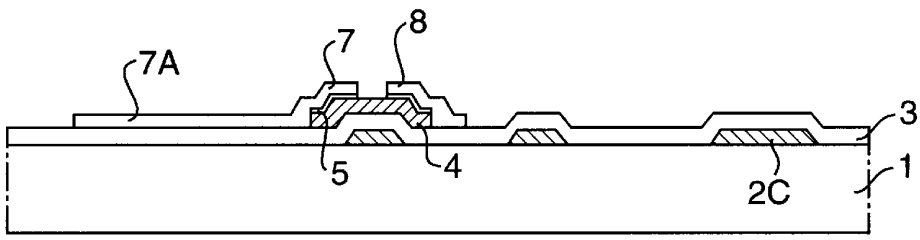


FIG. 2c

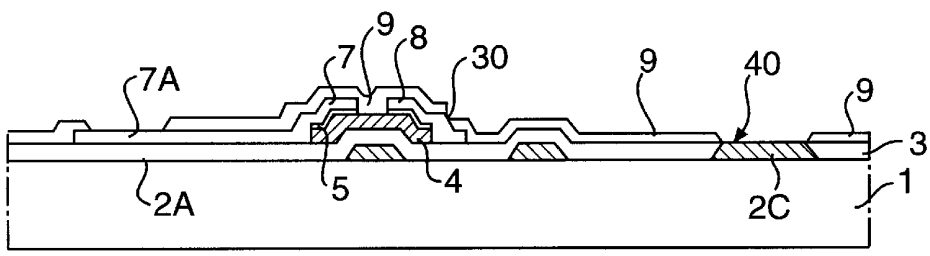


FIG. 2d

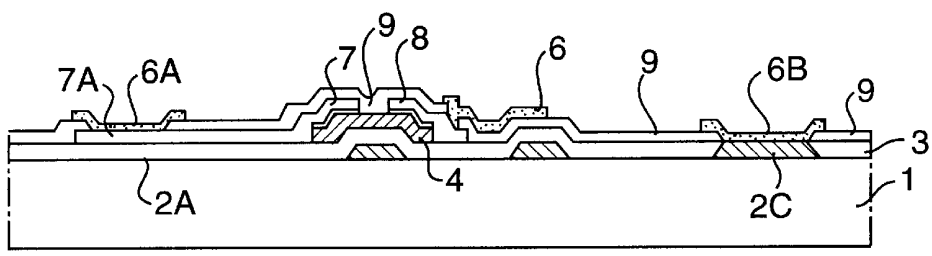


FIG. 2e

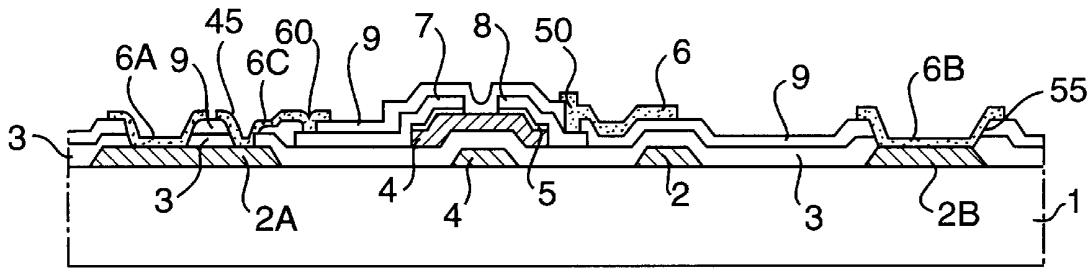


FIG. 3

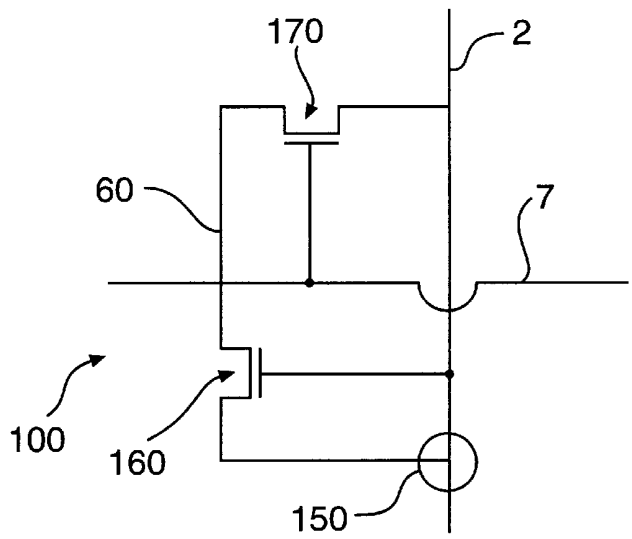


FIG. 4

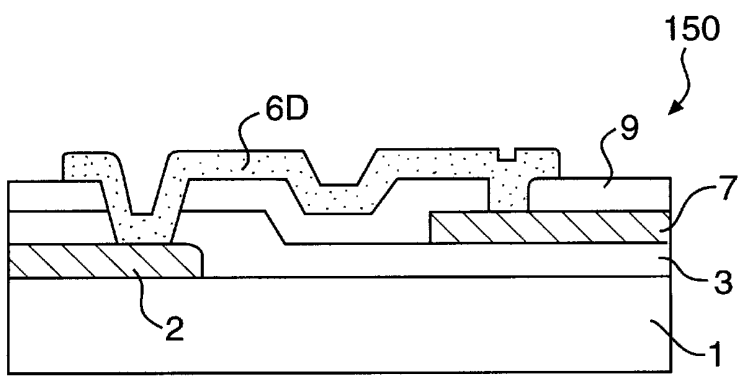


FIG. 5

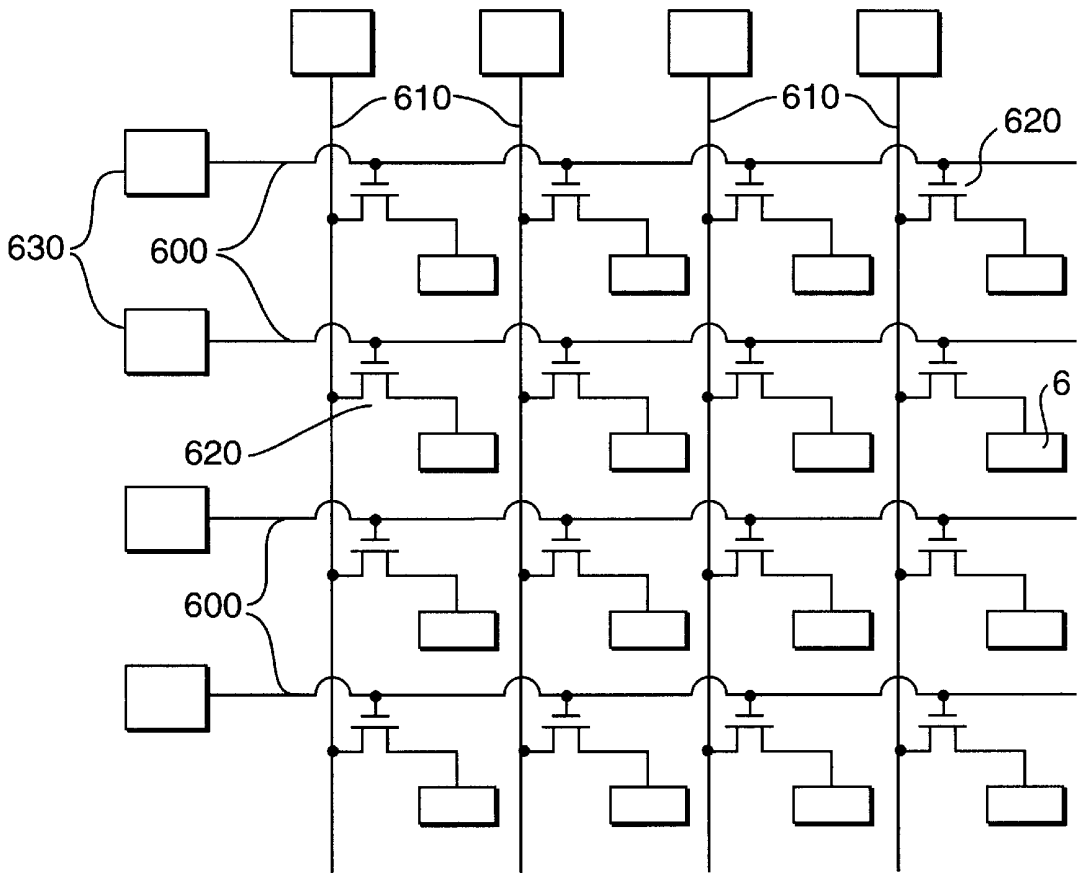


FIG. 6
PRIOR ART

LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME

This is a continuation of application Ser. No. 08/616,291, Filed Mar. 15, 1996.

BACKGROUND OF THE INVENTION

The present invention relates to a liquid crystal display (LCD) device and a method of manufacturing the same, and more particularly, to a liquid crystal display device having a combined source electrode and source pad structure.

Active matrix thin film displays include thin film transistors (TFTs) for driving the liquid crystal material in individual pixels of the display. As shown in FIG. **6**, a conventional LCD includes an array of pixels each having liquid crystal material (not shown) sandwiched between a common electrode provided on a top plate (not shown) and a pixel electrode **6** disposed on a bottom plate. The bottom plate further includes a plurality of gate lines **600** intersecting a plurality of data lines **610**.

Thin film transistors **620**, serving as active devices, are located at intersecting portions of gate lines **600** and data lines **610**. Gate lines **600** and data lines **610** are connected to the gates and sources, respectively of thin film transistors **620**. In addition, pixel electrodes **6** are connected to respective drain electrodes of thin film transistors **620**. Gate Pads **630** and Data Pads **640** are connected to the gate lines and data lines to receive datas from gate driver and data driver respectively.

A conventional method of manufacturing a liquid crystal display device including TFT driving elements will be described with reference to FIGS. **1***a*–**1***f*.

As shown in FIG. **1***a*, a conductive layer is formed on a transparent glass substrate **1** and patterned to form gate **2**, storage capacitor electrode **2**D, source pad **2**A, and gate pad **2**B. Gate pad **2**B is used for receiving a voltage to drive and active layer in the completed TFT device.

As shown in FIG. **1***b*, a gate insulating film **3**, such as a nitride film or an oxide film, is formed on the entire surface of the substrate in order to electrically insulate gate **2**. An amorphous silicon active layer **4** is formed on a portion of gate insulating film **3** overlying gate **2**. Then, in order to reduce the contact resistance between the active layer and the source/drain regions in the completed device, and appropriately doped semiconductor layer **5** is formed on amorphous silicon layer **4** as an ohmic contact layer. Doped semiconductor layer **5** and amorphous silicon layer **4** are then etched in accordance with a predetermined active layer pattern.

Since a pad wiring layer is necessary in order to communicate information from an external driving circuit to the gate and source, a gate insulating film **3** is selectively etched to expose source pad **2**A and gate pad **2**B (see FIG. **1***c*). Next, as shown in FIG. **1***d*, a transparent conductive layer (ITO) is deposited on the entire surface of the substrate and patterned to form a pixel electrode **6**, which is formed on a portion of the display pixel, while ITO patterns **6**A and **6**B are formed on source pad **2**A and gate pad **2**B, respectively.

As shown in FIG. **1***e*, the TFT is formed on the active layer and includes a conductive layer deposited on the substrate and simultaneously patterned to form source and drain electrodes **7** and **8**, respectively. Source electrode **7** is connected to source pad **2**A, and drain electrode **8** is contact with impurity-doped semiconductor layer **5** and pixel electrode **6**. In the completed device structure, source electrode **7** conducts a data signal, received from a data wiring layer and drain electrode **8**, to pixel electrode **6**. The signal is stored in the form of charge on pixel electrode **6**, thereby driving the liquid crystal.

As shown in FIG. **1***f*, a nitride film is deposited on the entire surface of the substrate as a passivation layer **9** in order to seal the underlying device from moisture and to prevent absorption of impurities. Passivation layer **9** is selectively etched to expose source-pad **2**A and gate pad **2**B, thereby completing the TFT.

In the conventional method described above, The source electrode **7** and pixel electrode **6** provided on the same surface of gate insulating film **3**. Accordingly, processing errors can cause these electrodes to contact each other. As a result, shorts can occur, thereby reducing yields.

Further, since the source pad for the source wiring is composed of the same material as the gate, its contact resistance with the underlying source electrode can be high. In addition, at least six masking steps are required as follows: patterning the gate, storage capacitor electrode, source pad and gate pad; forming the active layer pattern; patterning the gate insulating film for exposing the pad part; forming the pixel electrode; forming the source and drain electrode; and patterning the passivation film for exposing the pad part. Thus, the conventional process requires an excessive number of fabrication steps which increase cost and further reduce yield.

SUMMARY OF THE INVENTION

In order to solve the aforementioned problems, it is an objective of the present invention to provide a liquid crystal display device and a method of manufacturing the same, in which processing errors can be prevented and the Yield can be increased by etching the gate insulating film after the step of forming the passivation layer.

To accomplish this objective of the present invention, there is provided a liquid crystal display device comprising a substrate; a gate electrode; a gate pad and a source pad formed on the substrate as a first conductive layer; a gate insulating film formed on the entire surface of the substrate; a semiconductor layer and an impurity-doped semiconductor layer formed on the gate insulating film above the gate electrode; a source electrode and a drain electrode formed on the semiconductor layer; a passivation layer formed on the entire surface of the substrate; a first contact hole exposing the source pad; a second contact hole exposing a portion of the drain electrode; a third contact hole exposing the gate pad portion; and a fourth contact hole exposing the source electrode, the contact holes being formed by etching the passivation layer and gate insulating film; a pixel electrode connected with the drain electrode through the second contact hole; and a transparent conductive layer connecting the source pad with the source electrode through the first contact hole and fourth contact hole.

To further accomplish the objective of the present invention, there is also provided a method of manufacturing a liquid crystal display device, comprising the steps of forming a first conductive layer on a substrate; patterning the first conductive layer to respectively form a gate electrode, a gate pad and a source pad; sequentially forming an insulating film, a semiconductor layer and an impurity-doped semiconductor layer on the entire surface of the substrate; patterning the impurity-doped semiconductor layer and semiconductor layer to an active pattern; forming a second conductive layer on the entire surface of the substrate; patterning the second conductive layer to form a

source electrode and a drain electrode; forming a passivation film on the entire surface of the substrate; Selectively etching the passivation film and insulting film to respectively form a first contact hole exposing the source pad, a second contact hole exposing a portion of the drain electrode, a third contact hole exposing a gate pad portion, and a fourth contact hole exposing a portion of the source electrode; forming a transparent conductive layer on the entire surface of the substrate; and patterning a pixel electrode connected with the drain electrode through the second contact hole, a transparent conductive layer connected with the gate pad through the third contact hole, and a transparent conductive layer connecting the source pad with the source electrode through the first and fourth contact holes.

BRIEF DESCRIPTION OF THE ATTACHED DRAWINGS

FIG. **1***a* to if are cross-sectional views illustrating steps of a conventional method for manufacturing a liquid crystal display device;

FIGS. **2***a* to **2***e* are cross-sectional views illustrating steps of a method for manufacturing a liquid crystal display according to a preferred embodiment of the present invention;

FIG. **3** is a cross-sectional view illustrating a liquid crystal display device structure according to a second embodiment of the present invention;

FIG. **4** is a circuit diagram of one example of a liquid crystal display device in which a gate material is connected with a source material in accordance with a third embodiment of the present invention; and

FIG. **5** is a vertical-cross-sectional view of the device shown in FIG. **4**.

FIG. **6** is a plan view schemetic representation of one prior embodiment of a matrix display.

DETAILED DESCRIPTION OF THE INVENTION

Hereinafter, preferred embodiments of the present invention will be described with reference to the attached drawings.

Referring first to FIG. **2***a*, a conductive layer is formed on a transparent glass substrate **1** and patterned to form a gate electrode **2**, a storage capacitor electrode **2**D, and a gate pad **2**C, all of the same material. The gate electrode is used for applying a voltage in order to drive the active layer in the completed TFT device.

As shown in FIG. **2***b*, a gate insulating film **3** such as a nitride film or an oxide film is formed on the entire surface of the substrate in order to electrically insulate gate **2**. Semiconductor active layer **4** is then formed on insulating gate **2**. Active layer **4** is preferably made of amorphous silicon layer deposited by a chemical vapor deposition (CVD) process. Then, in order to reduce the contact resistance between the active layer and the subsequently formed source and drain, an impurity-doped semiconductor layer **5** is formed on amorphous silicon layer **4**, as an ohmic contact layer. Impurity-doped semiconductor layer **5** and amorphous silicon layer **4** are etched according to a predetermined active layer pattern.

As shown in FIG. **2***c*, a conductive layer for forming source electrode **7** and drain electrode **8** is deposited on the substrate by patterning a sputtered layer of conductive material. Using the source and drain electrodes as masks, portions of the impurity-doped semiconductor layer **5** are exposed and then etched. Source electrode **7** thus forms part of a transistor region and serves as source pad **7**A above the gate insulating film so that the same conductive layer constitutes part of the source wiring and the source electrode of the TFT.

As shown in FIG. **2***d*, a passivation layer **9**, e.g., a nitride film, is deposited on the entire surface of the substrate by a CVD process. Then, a predetermined portion of passivation layer **9** and gate insulating film **3** are selectively etched to form first, second and third contact holes **20**, **30** and **40**, thereby exposing a predetermined region of source pad **7**A above gate insulating film **3**, a predetermined region of drain electrode **8**, and a predetermined region of gate pad **2**C. For external electrical connections It is necessary to exposed pads **7**A and **2**C.

As shown in FIG. **2***e*, an indium tin oxide (ITO) layer is next deposited on the substrate by sputtering or a CVD process and etched according to a predetermined pattern to form a pixel electrode **6**. As further shown in FIG. **2***e*, pixel electrode **6** is connected to the upper portion of drain electrode **8** At the same time, ITO pattern **6**B is formed on gate pad **2**C. In addition, ITO pattern **6**A is provided on source pad **2**A, which is part of a data electrode of the LCD. The TFT of the present invention having electrical contacts or wiring structures including gate pad **2**C, layer **6**B and layer **6**A, source pad **7**A is thus completed.

As described above, the pixel electrode **6** is formed after the passivation process in the present invention. In contrast, pixel electrode **6** is formed after the pad process or the source/drain formation process in the conventional method. Thus, the passivation layer is interposed between the source/drain formation material and the pixel electrode, thereby effectively isolating these layers and preventing shorts.

Further, unlike the conventional process, the method in accordance with the present invention does not require the step of exposing the pad directly after depositing the gate insulating film, and the source and gate pads are exposed by etching during the passivation process. Thus, the pixel electrode, which is made of ITO, is formed on the source and gate pads. In addition, the source pad is not formed of gate material, but is formed from the source formation material, while the source and drain are deposited. Thus, the problem of high contact resistance between the source pad and the source, caused by forming the source pad from the gate material, can be avoided.

FIG. **3** illustrates a second embodiment of the present invention in which the step of etching the gate insulating layer and the step of etching the passivation layer to expose the pads are preformed in only one mask step. In particular, source pad **2**A is composed of gate material, as in the conventional method, and is formed at the same time as gate **2**, storage capacitor electrode **2**D and gate pad **2**B. After forming first, second, third and fourth contact holes **45**, **50**, **55** and **60**, material for forming the pixel electrode is then deposited. As a result, since both the first (**45**) and fourth (**60**) contact holes are formed over source pad **2**A (formed of the same material as the gate) and source electrode **7**, respectively, the source electrode **7** and source pad **2**A may be connected to each other in the same step that the pixel electrode is formed. Thus, after patterning, a first transparent conductive layer **6**C connects source electrode **7** with source pad **2**A, and a second transparent conductive layer **6** (i.e., the pixel electrode) is connected to drain electrode **8**.

In other words, a conductive layer is formed on a transparent glass substrate **1** and patterned to form gate **2**, a storage capacitor electrode **2**D,. a source pad **2**A and a gate

pad **2**B. After forming a gate insulating film **3** on the entire surface of the substrate, an amorphous silicon layer **4** and an impurity-doped semiconductor layer **5** are sequentially formed therson. These layers are then etched in accordance with a predetermined active layer pattern.

Then, a conductive layer is formed on the substrate and etched in accordance with a predetermined pattern, thereby forming a source electrode **7** and a drain electrode **8**. After forming a passivation layer **9** on the entire surface of the substrate, passivation layer **9** and gate insulating film **3** are selectively etched, thereby forming a first contact hole exposing the source pad **2**A and a third contact hole exposing the gate pad **2**B. Since the passivation layer **9** and gate insulating film **3** are preferably etched in a single step, the sidewalls of the first and second contact holes are planar and smooth.

ITO is then deposited on the entire surface of the substrate and patterned to form a pixel electrode **6** connected to drain electrode **8** through the contact hole overlying drain electrode **8** in the pixel part. At the same time, ITO patterns **6**A, **6**B and **6**C are formed to contact source pad **2**A and gate pad **2**B through the contact holes formed at gate insulating film **3** and passivation layer **9**.

Further, in accordance with an additional embodiment of the present invention, a repair line or static electricity protection circuit can also be provided during deposition of the pixel electrode layer. FIG.**4** is a schematic diagram of static electricity protection circuit **100**, and FIG.**5** is an enlarged cross-sectional view of a portion **150**,of the circuit.

In the circuit shown in FIG.**4**. if a high potential due to an electrostatic discharge is present on source electrode **7**, for example, transistor **170** is rendered conductive to discharge source electrode **7** to gate line **2**. Similarly, gate line **2** can discharge to source electrode **7** via transistor **160**. As shown in FIG.**5**, the connection between gate line **2** and source electrode **7** is achieved by forming contact holes in insulative films **3** and **9** and then depositing conductive material (preferabel ITO) into these holes while forming the pixel electrode.

According to the present invention as described above, the manufacture of the TFT of the liquid crystal display device can be accomplished using five mask steps (step of forming the gate, step of forming the active layer, step of forming the source and drain, step of etching the passivation layer and gate insulating film, and step of forming the pixel electrode), while the conventional process requires six or more mask steps. Thus, manufacturing cost can be reduced.

Further, when the source pad is formed from the same material as the source electrode, the contact resistance problem caused when the source pad is in contact with the source electrode can be solved. In addition, since the pixel electrode is formed after forming the passivation layer, processing errors resulting in the pixel electrode contacting the source and drain can be prevented.

Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

What is claimed is:

1. A wiring structure comprising:

a substrate;

a first conductive layer formed on a first portion of said substrate;

a first insulative layer formed on a second portion of said substrate and on said first conductive layer;

a second conductive layer formed on a first portion of said first insulative layer;

a second insulative layer formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer;

an indium tin oxide layer formed on said second insulative layer,

wherein a first contact hole is provided through said first and second insulative layers to expose part of said first conductive layer and a second contact hole is provided through said second insulative layer to expose part of said second conductive layer, said indium tin oxide layer extends through said first and second contact holes to electrically connect said first conductive layer with said second conductive layer, and

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

2. A wiring structure comprising:

a substrate;

a first conductive layer formed on a portion of said substrate;

a first insulative layer having a first via hole exposing a portion of said first conductive layer;

a second conductive layer formed on a portion of said first insulative layer;

a second insulative layer having a second via hole exposing said exposed portion of the first conductive layer and having a third via hole exposing a portion of the second conductive layer;

a third conductive layer formed on said second insulative layer and electrically connecting said first conductive layer to said second conductive layer through said first, second, and third via holes,

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

3. A wiring structure in accordance with claim **2**, wherein said third conductive layer includes indium tin oxide.

4. A wiring structure in accordance with claim **2**, wherein said first and second via holes constitute a common hole exposing said exposed portion of said first conductive layer, a sidewall of said common hole being substantially smooth.

5. A wiring structure in accordance with claim **2**, wherein said second via hole is aligned with said first via hole.

6. A liquid crystal display device comprising:

a substrate having a primary surface;

a first conductive layer disposed on a predetermined region of said primary surface;

a first insulating layer formed overlying said primary surface including said first conductive layer, said first insulating layer including a first contact hole exposing a predetermined portion of said first conductive layer;

a second conductive layer formed on a predetermined region of said first insulating layer;

a second insulating layer formed overlying said primary surface including said second conductive layer, said second insulating layer having a second contact hole exposing a predetermined portion of said second conductive layer and said first contact hole region; and

a third conductive layer formed on said second insulating layer and electrically connected to said first and second conductive layers via said first and second contact holes,

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

7. A liquid crystal display device in accordance with claim **6**, wherein said third conductive layer includes material suitable for forming a pixel electrode.

8. A method of manufacturing a liquid crystal display device, comprising the steps of:

forming a first conductive layer pattern on a substrate, said first conductive layer pattern being connected to a first terminal of a thin film transistor;

forming a first insulating layer overlying a surface of said substrate including said first conductive layer pattern;

forming a second conductive layer pattern on said first insulating layer, said second conductive layer pattern being connected to a second terminal of the thin film transistor;

forming a second insulating layer overlying said substrate including said second conductive layer pattern;

selectively etching said first and second insulating layers to form a first contact hole and a second contact hole exposing said first conductive layer pattern and said second conductive layer pattern, respectively; and

forming a third conductive layer on said second insulating layer, said third conductive layer electrically connected to said first and second conductive layer patterns via said first and second contact holes, respectively.

9. A method of manufacturing a liquid crystal display device in accordance with claim **8**, wherein said selective etching step is performed in a single etch step and said third conductive layer includes indium tin oxide.

10. A liquid crystal display device comprising:

a substrate;

a first conductive layer on said substrate including:
a gate electrode,
a gate pad, and
a source pad;

a gate insulating film on said surface of said substrate,

a portion of said gate insulating film overlying said gate electrode;

a semiconductor layer on said portion of said gate insulating film;

an impurity-doped semiconductor layer on said semiconductor layer;

a source electrode and a drain electrode on said semiconductor layer;

a passivation layer overlying said source pad, said drain electrode, said gate pad, and said source electrode;

a first contact hole provided through said passivation layer and said gate insulating film exposing said source pad;

a second contact hole provided through said passivation layer exposing said drain electrode;

a third contact hole provided through said passivation layer and said gate insulating film exposing said gate pad;

a fourth contact hole provided through said passivation layer exposing said source electrode;

a pixel electrode electrically connected with said drain electrode via said second contact hole; and

a transparent conductive layer electrically connecting said source pad with said source electrode via said first contact hole and said fourth contact hole.

11. A method of manufacturing a liquid crystal display device, comprising the steps of:

forming a first conductive layer on a substrate;

patterning said first conductive layer to form a gate electrode, a gate pad and a source pad;

forming an insulating film on said substrate including said patterned conductive layer;

forming a semiconductor layer on said insulating film;

forming an impurity-doped semiconductor layer on said semiconductor layer;

patterning said impurity-doped semiconductor layer and said semiconductor layer to form an active layer;

forming a second conductive layer overlying said substrate including said active layer;

patterning said second conductive layer to form source electrode and a drain electrode on said active layer;

forming a passivation film overlying said substrate including said source pad, a portion of said drain electrode, said gate pad portion, and a portion of said source electrode;

selectively etching said passivation film and said insulating film to form a first contact hole exposing said source pad, a second contact hole exposing said portion of said drain electrode, a third contact hole exposing said gate pad portion, and a fourth contact hole exposing said portion of said source electrode;

patterning a pixel electrode electrically connected to said drain electrode via said second contact hole;

patterning a first transparent conductive layer electrically connected to said gate pad through said third contact hole; and

patterning second transparent conductive layer electrically connecting said source pad to said source electrode via said first and fourth contact holes.

* * * * *

EXHIBIT D

Moving back to the lab, the next step will be to understand in molecular detail where survival pathways and chemotherapy agents intersect. ■

Frank McCormick is at the Comprehensive Cancer Center, University of California, San Francisco, Box 0128, 2340 Sutter Street, San Francisco, California 94143, USA.
e-mail: mccormick@cc.ucsf.edu

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Semiconductor physics

Quick-set thin films

Mercouri G. Kanatzidis

Transistors that have active components based on thin films, rather than silicon, are attractive for many applications. The latest thin-film fabrication technique has the potential for industrial-scale production.

The original working transistor, invented at Bell Labs in the 1940s, was based on semiconducting germanium and had a junction (sandwich) configuration. But by the 1960s, this design had given way to the simpler field-effect transistor — in particular, the silicon-based MOSFET (for metal-oxide-semiconductor field-effect transistor). A typical computer processor today contains around 42 million such transistors, and demand for ever-faster computers is only increasing. As a result, the market is pushing for a downsizing of transistor technology.

However, certain applications (such as flat-panel displays) require larger-area transistors than can normally be created using silicon-based devices. Thin-film semiconductors have been explored as an alternative, although with limited success. But now it seems that the large-scale, low-cost fabrication of such devices is a step closer: on page 299 of this issue, Mitzi *et al.*[1] describe a chemical-deposition method for producing uniform films of the chalcogenides SnS_2 or $SnSe_2$ for use in thin-film transistors (TFTs). The resulting TFTs support large current densities (more than 10^5 A cm^{-2}), and mobilities greater than 10 cm^2 V^{-1} s^{-1} — almost ten times larger than achieved for semiconducting films formed using the spin-coating technique (in which a solution on a substrate is spun rapidly, causing the film to spread outwards).

In a TFT, the thin film (usually silicon) is the active current-carrying layer (Fig. 1). The film sits on a substrate, which is usually glass owing to its low cost, high optical transparency and compatibility with conventional semiconductor processing technology. Recently, however, plastic has emerged as a viable challenger because of its additional flexibility, although the development of TFT technology for use with plastic substrates is still in its infancy.

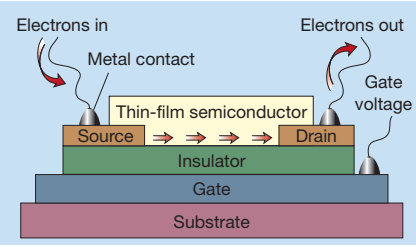

Figure 1 **Cross-section of a thin-film transistor. A voltage applied at the gate controls the flow of electrons (resistance) from the source to the drain; a positive gate voltage attracts electrons to the bottom surface of the semiconductor layer and creates a conduction channel. When a voltage difference is applied between the two connector wires, electrons enter at one end (the source) and exit at the other (the drain), resulting in a current along the channel. Mitzi *et al.*[1] have now come up with a chemical-deposition method that produces uniform films of the chalcogenide $SnSe_2$ for use in thin-film transistors.**

Transistors for high-performance display applications should have high electron mobilities, low leakage currents and low threshold voltages. But processing temperatures must also be low (below 150 °C) if the transistors are to be compatible with low-cost plastic substrate materials. So the emphasis in developing large-scale TFTs has been on low-temperature deposition and the exploration of materials other than amorphous silicon. Approaches include vacuum deposition[2] (suitable for growing ultrathin organic films and multilayer structures), solution-deposition technologies[3] (suitable for inorganic materials), and many others[4]. But these are generally not high-throughput processes. Although spin-coated semiconductor films have suffered from low mobilities[5–7], this technique shows much promise.

The attraction of using inorganic semiconductors lies in their stability, thermal robustness and high mobilities. The metal chalcogenides, for example, are excellent candidates for use in TFT technologies. They form a large class of compounds that are composed of one or more metals plus one of the chalcogen atoms such as sulphur, selenium or tellurium. Moreover, the energy required to delocalize a charge carrier (the energy gap)[8] in these materials is suitable for room-temperature devices, and can be further tuned for a given application[9].

Mitzi *et al.*[1] describe a means of creating chalcogenide active layers for TFTs through spin coating. Their continuous, uniform, ultrathin semiconducting films are only a few unit cells thick. The key to the fabrication chemistry is hydrazine (N_2H_4), which Mitzi *et al.* use as a solvent. When metal and chalcogens dissolve in hydrazine, they form chalcogenometallate solutions containing anions such as $[Sn_2S_6]^{4-}$, as well as hydrazinium cations $(N_2H_5)^+$. These solutions can be used as precursors for spin-coating thin films of the salt $(N_2H_5)_4[Sn_2S_6]$, which then decompose to the binary metal chalcogenide at low temperature. The advantage of having hydrazinium cations, and not some other organic cations[10], is that they readily and cleanly react with the counterion of $[Sn_2S_6]^{4-}$ to give continuous, crystalline semiconducting films as thin as 5 nanometres.

It is this simple chemistry that not only makes the work of Mitzi *et al.*[1] attractive, but probably technologically significant as well. Thin films produced by deposition from solution have so far been moderately successful in terms of their mobilities[11–13], but the techniques are generally not suitable for high throughput. This hydrazine-based process can be applied more generally, and the hydrazinium salts need not be isolated first — they can be made *in situ*. If the process can be optimized and scaled up, thin films for high-performance channel layers in TFTs could be fabricated with all the processing performed at 300 °C. In principle, depending on the specific metal chalcogenide involved, the films could be made at even lower temperatures.

However, the current processing temperature is too high for many applications (such as those using plastic substrates), and the mobilities achieved, although much higher than reported for other techniques, may not yet be adequate for many devices. Furthermore, the source and gate voltages of the TFTs are higher than those of typical silicon-based devices, while little is known about the yield and reproducibility of these devices. And the substrate is still silicon, not glass or plastic, which will limit the fabrication of TFTs on large-area, low-cost substrates.

So there are several factors to be considered before a new generation of opto-electronic devices based on this deposition

technology could gain a foothold, including the long-term operational and environmental stability of the devices. But, given the relative youth of this technology, and the exciting and rapid advances anticipated using chalcogenide thin films, the goal does not seem unattainable. Continued work in this area is likely to contribute to our understanding and exploitation of these exciting materials well into the next century. ■

Mercouri G. Kanatzidis is in the Department of Chemistry, Michigan State University, East Lansing, Michigan 48824, USA.
e-mail: kanatzidis@chemistry.msu.edu

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Cancer

Dangerous liaisons

Allan Balmain and Rosemary J. Akhurst

The cells of multicellular organisms are highly communicative and so can strongly influence one another's behaviour. One line of communication is particularly important in keeping cell growth in check.

A single cell destined to become a tissue or an organism can't go it alone in its rise to such dizzy heights. Communication, in the form of direct contacts between cells, interactions between cells and their surroundings, or the transmission of biochemical signals, is essential. Unravelling these networks of communication has provided gainful employment for biologists, geneticists and mathematicians in their quest to understand how the body forms[1]. But now cancer biologists are being drawn into a similar web of interactions between cells targeted to become tumours (usually epithelial cells) and their neighbours (stromal fibroblasts). A network of signals operates in tumours. As they describe in *Science*, Bhowmick *et al.*[2] have identified one signalling pathway — regulated by transforming growth factor β (TGF-β) — that is an important mediator of the stromal–epithelial interactions modulating the growth of solid tumours.

It has been known[3] for some years that normal stromal cells inhibit tumour growth whereas tumour-associated stromal cells stimulate it (Fig. 1). In their study, Bhowmick *et al.*[2] deleted the receptor for TGF-β — the TGF-β type II receptor — specifically in stromal cells of otherwise normal mice. This 'selective knockout' avoided killing the animals by deleting the TGF-β type II receptor in every cell type, completely inhibiting signalling through this pathway in the stroma of several tissues. Surprisingly, although the deletion occurs in the skin, oesophagus, kidney, liver and lung, mice were born normally, and these tissues showed no observable adverse effects.

Not everything, however, escaped unscathed. Prostate tissue underwent increased stromal-cell division, growing excessively by the time the animals were three weeks old. This, in turn, stimulated the epithelial cells of the prostate to divide and form lesions that resembled prostatic intraepithelial neoplasia, a probable forerunner of prostate cancer. The stromal-cell population in the animals' forestomach also proliferated more rapidly, in this case spurring the expansion of the epithelial population so that an invasive form of cancer occurred that killed the mice by the time they were seven weeks old. So not only does abrogation of TGF-β signalling in the stromal fibroblasts cause them to proliferate, but the ensuing perturbed communication with the epithelial cells causes dysregulated cell division, indirectly leading to cancerous growth.

What causes this? Perhaps the stromal cells that cannot respond to TGF-β instead release other factors, or greater amounts of certain factors than do normal stromal cells? Bhowmick *et al.*[2] suggest that it might be due to another growth factor, hepatocyte growth factor (HGF), acting through its receptor c-Met (Fig. 1). The HGF–c-Met regulatory system is important in proliferation, cell migration and metastasis — the movement of cancer cells to other parts of the body to establish more tumours[4]. Impressively, fibroblasts from both the forestomach and prostate tissues of the knockout mice secreted at least three times as much HGF as their normal counterparts, and c-Met was simultaneously activated in the proliferating epithelial cells of the forestomach tumours.

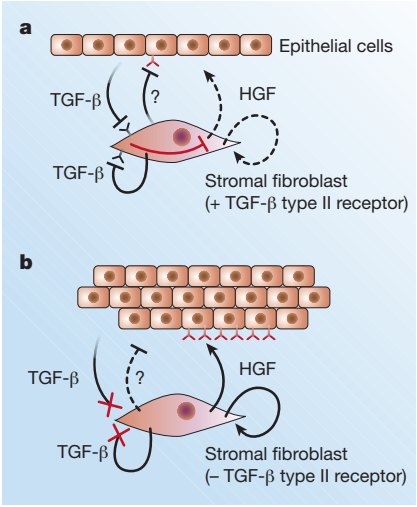

Figure 1 **Cellular relationships.** a, **Normal communications between epithelial cells and their fibroblast neighbours. Both epithelial cells and fibroblasts secrete transforming growth factor β (TGF-β), which suppresses growth. Stromal fibroblasts might also secrete other factors that inhibit epithelial-cell growth (denoted by ?). A small amount of hepatocyte growth factor (HGF; its receptor is c-Met) secreted by the stroma inhibits stromal-cell growth and also that of epithelial cells.** b, **Perturbed signalling in the absence of the receptor for TGF-β, the TGF-β type II receptor. Inhibition of TGF-β signalling in stromal cells prevents growth-inhibitory responses to TGF-β and stimulates the stroma to release higher levels of HGF, a positive growth and metastatic factor. The production of other growth-inhibitory factors (?) might be reduced in response to inhibition of TGF-β signalling. TGF-β receptors are shown in black, c-Met receptors in red.**

These data are consistent with previous reports that TGF-β normally inhibits HGF synthesis in stromal cells[5]. But they don't reflect the situation in advanced skin cancer, in which tumour-derived TGF-β induces adjacent stromal cells to produce HGF[6].

The study by Bhowmick and colleagues has uncovered insights into cellular liaisons within tissues that should benefit cancer researchers and developmental biologists alike. But several issues raised by the findings must first be resolved. The cells of most solid tumours secrete large amounts of TGF-β, but are insensitive to its growth-inhibitory effects. This means either that components of this signalling pathway have mutated or, as is more common, that the growth response has been reduced while the ability to migrate, invade and metastasize in response to TGF-β is retained. How, then, do stromal cells normally escape the growth-inhibitory effects of overexpressed TGF-β and become willing partners in fostering epithelial tumour progression? Possible answers are genetic changes, or changes in gene expression that occur without altering the DNA sequence.

EXHIBIT E

United States Patent [19]

Morin et al.

[11] **4,343,081**

[45] **Aug. 10, 1982**

[54] **PROCESS FOR MAKING SEMI-CONDUCTOR DEVICES**

[75] Inventors: **Francois Morin**, Lanmerin; **Madeleine Bonnel**, Lannion, both of France

[73] Assignee: **L'Etat Francais represente par le Secretaire d'Etat aux Postes et Telecommunications et a la Telediffusion (Centre National d'Etudes des Telecommunications)**, Issy les Moulineaux, France

[21] Appl. No.: **160,213**

[22] Filed: **Jun. 17, 1980**

[30] **Foreign Application Priority Data**

Jun. 22, 1979 [FR] France 79 16083
Dec. 18, 1979 [FR] France 79 30954

[51] **Int. Cl.**[3] **H01L 21/225**

[52] **U.S. Cl.** **29/571**; 148/187; 148/188

[58] **Field of Search** 29/571; 357/23; 148/174, 188, 187

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Primary Examiner—G. Ozaki
Attorney, Agent, or Firm—Pearne, Gordon, Sessions, McCoy & Granger

[57] **ABSTRACT**

The present invention relates to a process for making semi-conductor components on an amorphous substrate, comprising two phases, wherein, in a first phase, the substrate is introduced into a deposition chamber and a uniform deposit is made of four successive primary layers on all this substrate, without contact with the outside atmosphere: a first layer of protective insulating material, a second layer of semiconductor material, a third layer of insulating material, of smaller thickness than the first layer, and finally a fourth layer of a metal; and, in a second phase, the substrate coated with these four layers is withdrawn from the deposition chamber and the last three layers are subjected to photoetching and ancillary deposition operations, which are appropriate for the structure of the component to be obtained.

5 Claims, 11 Drawing Figures

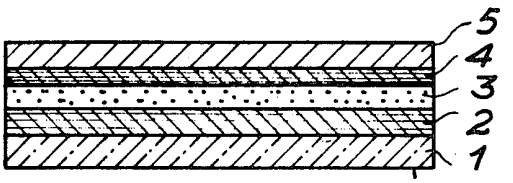
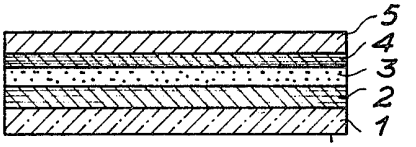


FIG.1



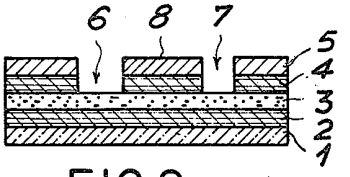


FIG.2a

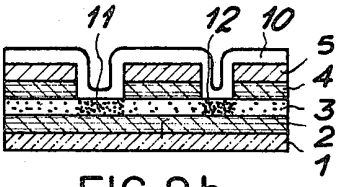


FIG.2b

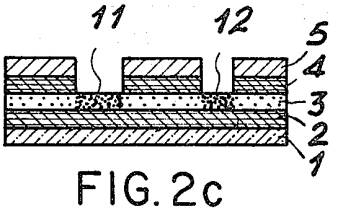


FIG.2c

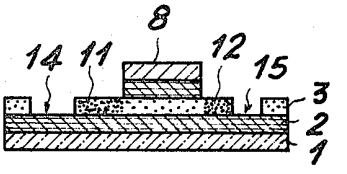


FIG.2d

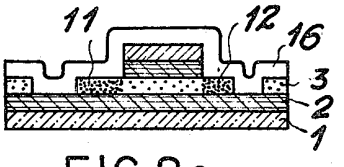


FIG.2e

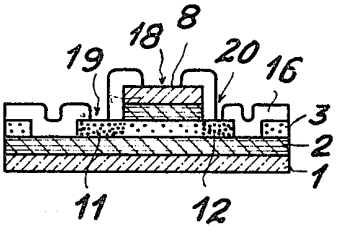


FIG.2f

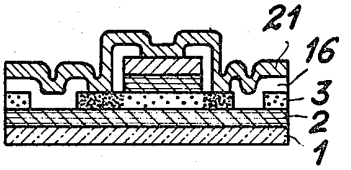


FIG.2g

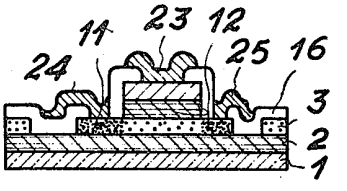


FIG.2h

FIG.3

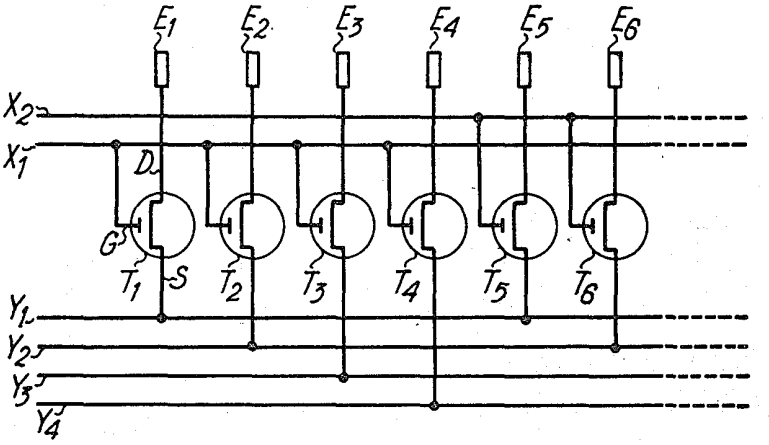

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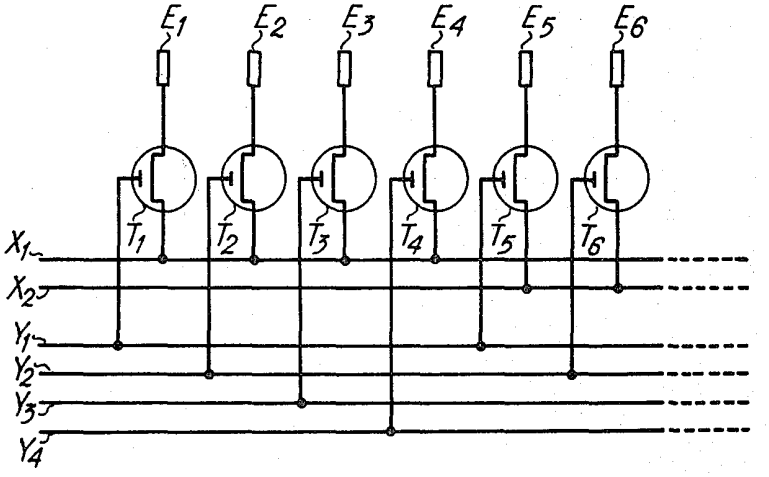
FIG.4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X2
Y1
Y2
Y3
Y4

FIG.5a

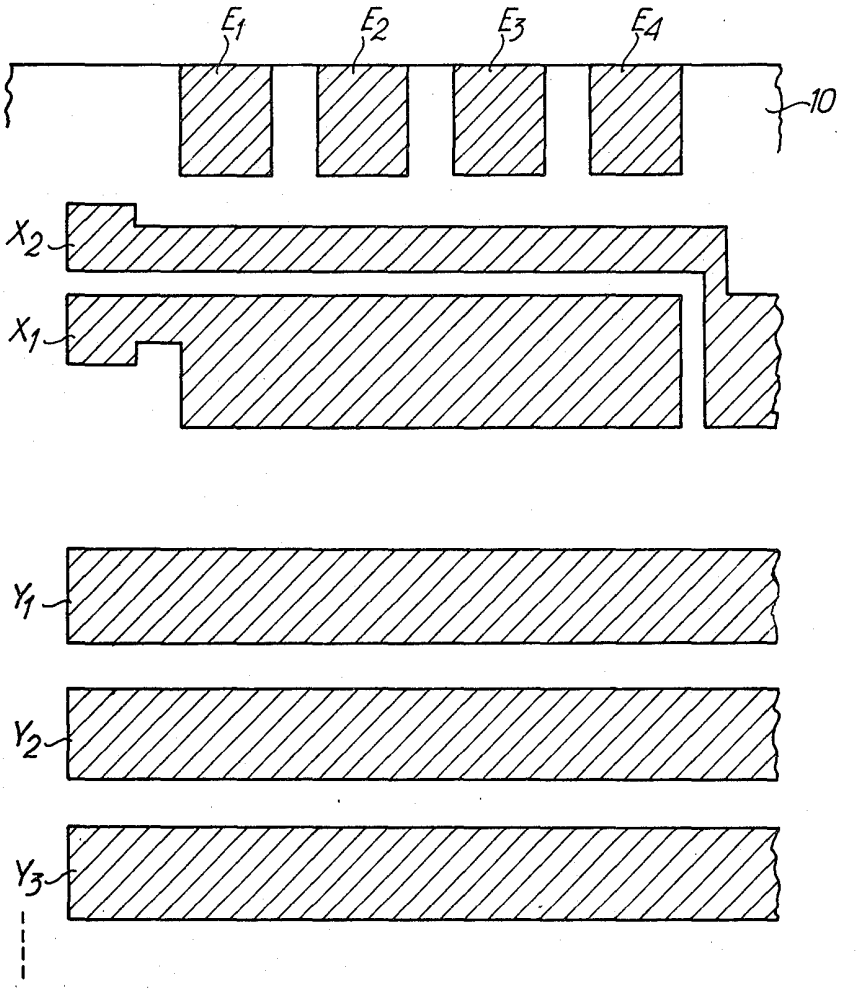


FIG.5b

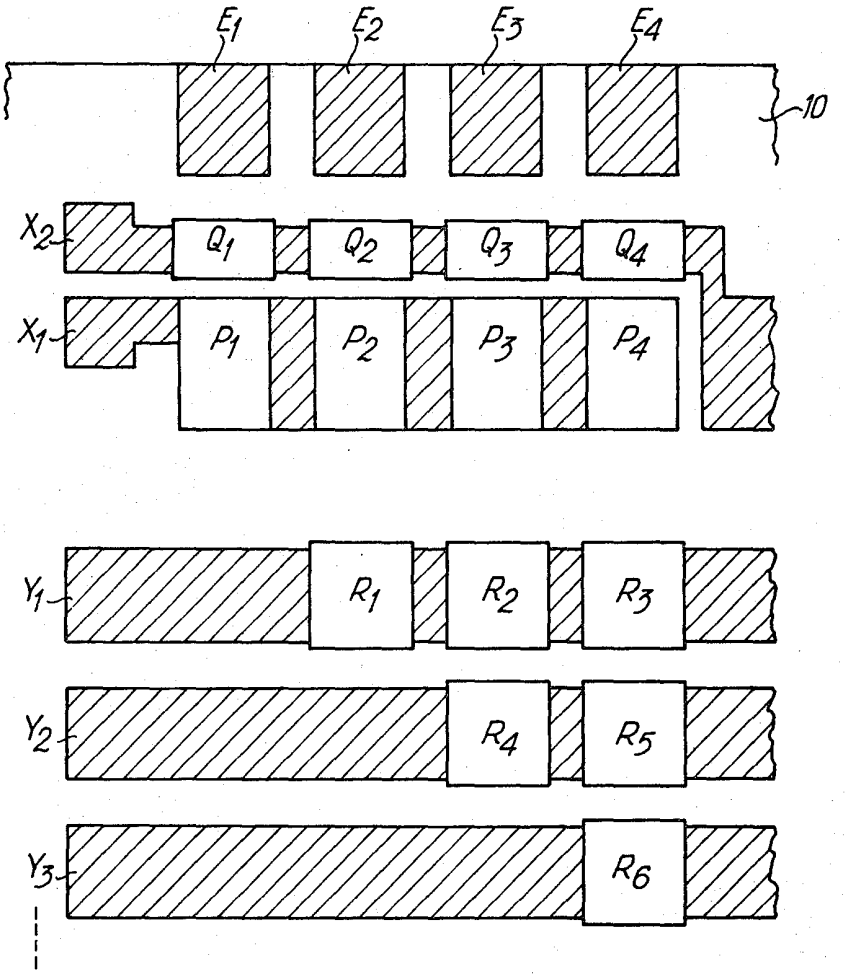


FIG.5c

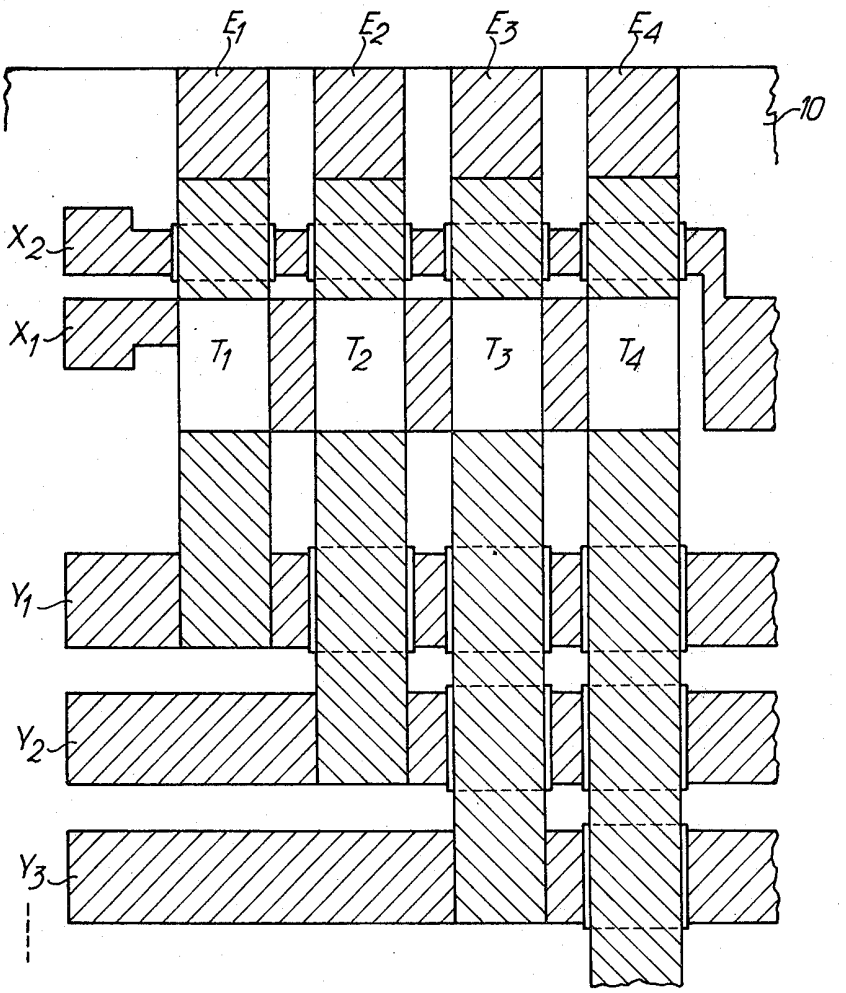


FIG.6a

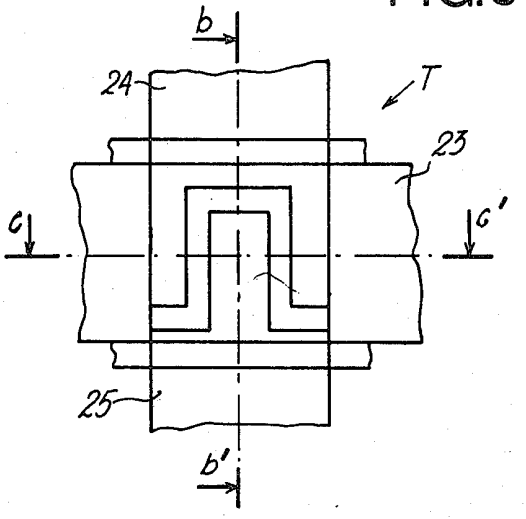


FIG.6b

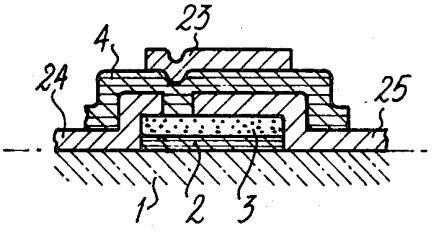


FIG.6c

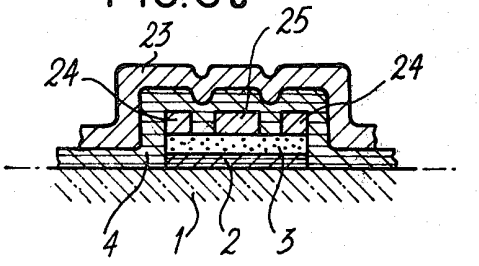
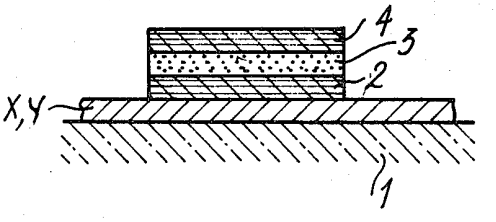


FIG.7



PROCESS FOR MAKING SEMI-CONDUCTOR DEVICES

The present invention relates to a process for making semi-conductor components and to a component obtained by this process. It finds particular application in the production of thin-film transistors (hereinafter abbreviated to T.F.T.s) and of circuits using T.F.T.s.

A T.F.T. is a field effect transistor with insulated grid. It is similar to an MOS (metal-oxide semiconductor) transistor, with the difference that it is made on an amorphous substrate and not on a monocrystalline silicon wafer. Consequently, T.F.T. circuits may be of very large dimensions and are no longer limited by the size of the crystalline substrate.

In practice, a T.F.T. is obtained by deposit in vacuo of its different constituents on a glass substrate. Each layer (semiconductor, insulator, metal) is deposited through a metal mask (of the Stencil-mask type) in intimate contact with the substrate. To have a good definition of the patterns, the deposits are made by evaporation in vacuo. The materials to be evaporated are disposed in crucibles heated by the Joule effect or by electron bombardment. The in-situ masking excludes deposits in a gaseous atmosphere (cathode sputtering, chemical deposit by gaseous process, etc.) because of the sheath phenomena which render the edges of the patterns blurred. In the best of cases, an in vacuo mask exchanger enables all the T.F.T. (or T.F.T. circuit) to be made in one pumping cycle, this avoiding pollution of the semiconducting layer and of the insulator-semiconductor interface.

Concerning this technique and applications thereof, the article by A. G. Fischer entitled 'Flat TV panels with polycrystaline layers' published in the journal 'Microelectronics', Vol. 7, No. 4, 1976, pages 5 to 15, may be consulted.

Although the main advantage of this technique of making T.F.T.s is a rapid execution of the circuits, it has the drawback of being suitable only for circuits of modest dimensions and definition. In fact, a metal mask of high definition and large outer dimensions comprises a large number of very small openings, has mediocre mechanical properties, expands, and deforms. As a plurality of masks are necessary and as the patterns must be superimposed with high precision, a limitation is rapidly apparent. It is estimated that this method enables circuits of overall dimensions of the order of about ten centimeters to be produced, not having more than four transistors per square millimeter. These modest performances limit the applications of the T.F.T.

Furthermore, this technique imposes that the layers constituting the transistor be disposed on a substrate at ambient temperature, in order to avoid the expansion of the masks. Now, the semiconductor deposit which is generally polycrystalline, would necessitate the use of a much higher substrate temperature (a few hundred degrees) in order to improve crystallization.

Other processes of manufacture have been developed, employing partial photoetching of the layers. They have the drawback of polluting the semiconductor layer in its active part. A description of these processes will be found in the article by J. C. Erskine and A. Cserhati entitled 'Cadmium selenide thin-film transistors' published in the journal 'Journal of Vaccum Science Technology', Vol. 15(6), Nov./Dec. 1978, pages 1823 to 1835.

It is an object of the present invention to provide a process for manufacturing semiconductor components and particularly T.F.T.s, which avoids all these drawbacks. The process of the invention employs the principle of photoetching whilst conserving one of the advantages of the process described hereinabove, namely the production of all the layers constituting the T.F.T. in one manufacturing cycle, thus avoiding the pollution of the layers and interfaces by outside agents. However, the invention has the following advantages over the known process:

1. The substrate may be heated during the deposit of the semiconductor, this leading to an improvement in the crystallization.

2. The dimensions of the substrate may be as large as is desired, within the limit of the homogeneity of the deposits.

3. The deposition techniques are no longer limited to evaporation is vacuo and cathode sputtering, chemical deposit by gas process, etc. may be used.

4. The definition of the patterns is increased by the use of photographic masks of high precision, already used for making integrated circuits.

5. The complexity of the circuits made is greater and attains that of integrated circuits.

6. The process of photoetching described hereinbelow effects the self-alignment of the grid on the channel of the T.F.T., this eliminating the parasitic grid-source and grid-drain capacitances.

To this end, the process according to the invention comprises two phases:

(A) in a first phase,
- the substrate is introduced into a deposition chamber,
- a uniform deposit of four successive primary layers is made on all this substrate, without contact with the outside atmosphere: a first layer of protective insulating material, a second layer of semiconductor material, a third layer of insulating material, of smaller thickness than the first layer, and finally a fourth layer of a metal,

(B) and, in a second phase:
- the substrate coated with these four layers is withdrawn from the deposition chamber,
- the last three layers are subjected to photoetching and ancillary deposition operations, which are appropriate for the structure of the component to be obtained.

The invention will be more readily understood on reading the following description with reference to the accompanying drawings, in which:

FIG. **1** shows a schematic section of the substrate obtained after the first phase,

FIG. **2** shows a schematic section of the structure obtained at various stages of the second phase,

FIG. **3** schematically shows a multiplexed T.F.T. control circuit for a teleprinter restitution head, according to a first embodiment,

FIG. **4** schematically shows a multiplexed T.F.T. control circuit for a teleprinter restitution head, according to a second embodiment,

FIGS. **5***a*, **5***b* and **5***c* schematically show, in plan view, three stages of manufacture of the control circuit,

FIG. **6** shows a T.F.T. in plan view (a) and in transverse sections (b) and (c).

FIG. **7** shows a crossing zone in section.

Referring now to the drawings, FIG. **1** shows in schematic section (neither the proportion nor the dimensions are respected) a substrate **1** on which are

deposited; a thick layer **2** of insulating material, a layer **3** of semiconductor, a thin layer **4** of insulator and finally a layer **5** of metal. The operating conditions relative to this first phase may be as follows:

The substrate **1** on which it is desired to make the T.F.T. circuit is firstly introduced into a deposition chamber. Four successive deposits are made, without contact with the outside atmosphere:

1. Deposit of the thick insulating layer **2**

To protect the circuit from the impurities which may be contained in the substrate, a thick insulating layer **2** is firstly deposited, after degassing. This layer will serve as barrier for the alkaline ions which might diffuse in the semiconductor and deteriorate it. A layer of alumina deposited by evaporation of sapphire employing an electron gun may for example be used.

2. Deposit of the semiconductor film **3**

For this operation, the substrate is taken to as high a temperature as possible (generally a little below 500° C. if the substrate is made of glass). In the example described here, the semiconductor is cadmium selenide—CdSe—deposited by evaporation in vacuo. The temperature of the substrate is maintained at 400° C. during the deposition.

3. Deposit of the thin insulating layer **4**

The grid insulator is then deposited. The power of modulation of the grid depends on its dielectric qualities. Its thickness will determine the breakdown voltage of the transistor. In the example described here, a thin layer of alumina, prepared as in **1**, is used.

4. Deposit of the grid metal **5**

Molybdenum evaporated with an electron gun may be used.

At this stage, the deposits may undergo an appropriate thermal treatment: annealing in vacuo or in a special atmosphere.

After it has been removed from the deposition chamber, the substrate, on which the four primary layers have just been deposited, is then subjected to the operations of photoetching and ancillary deposits appropriate for the second phase.

Photoetching consists in using a photosensitive resin, sensitized to ultra-violet light, through a photographic mask reproducing the desired pattern. After development and hardening of the resin, the exposed parts are eliminated by chemical etching. After etching, the protective layer of resin may easily be removed by dissolution in a suitable solvent.

This technique is currently used in the manufacture of integrated circuits and transistors, but, in the present case, the steps of the process of manufacture are different and original. They are illustrated in FIG. **2**, which shows eight sections a, b, c, d, e, f, g, and h, corresponding to the following eight phases:

(a) Photoetching of the metal layer **5** and the insulating layer **4** with the aid of a first mask. This first photoetching makes windows **6** and **7** on the semiconductor and defines the grids **8** of the T.F.T.s. In the example described here, the molybdenum and alumina not protected by the resin are selectively attacked by immersion in acid solutions.

(b) Deposit of a diffusing metal **10** and diffusion thereof by annealing. This diffusion renders the parts **11** and **12** of the semiconductor **3** defined in (a) conducting; the diffusing metal may be aluminum or chromium, and may diffuse towards 400° C.

(c) Elimination of the excess metal by chemical attack, which must be selective, since it must leave the grid metal **5** intact.

(d) With the aid of a second mask, photoetching of the semiconductor layer in order to create windows **14** and **15** which insulate the components on the substrate. In the example taken, the cadmium selenide may be eliminated by a solution of bromine-ethanol.

(e) Deposit of a thick insulator **16**, different from insulators **1** and **4**. This may, for example, be SiO_2.

(f) With the aid of a third mask and a selective chemical attack, opening of windows **18**, **19** and **20** in the thick insulator, in order to be able to make contacts on the grid **8**, source **11** and drain **12** of each transistor.

(g) Deposit of a layer **21** of contact metal. This metal may, for example, be aluminum.

(h) With the aid of a fourth mask, photoetching of the contacts. Contact **23** of the grid, **24** of the source and **25** of the drain are then obtained.

The process of manufacture which has just been described, by the advantages that it procures, extends the field of application of the T.F.T. The possibility of making circuits of large dimensions (the limit is imposed by the homogeneity of the deposits and the capacity of the mask aligner, but the production of circuits of several square decimeters may be envisaged) enables circuits to be designed for controlling flat screens, directly on the support of the screen, this solving the problems of connection. The high resolution of the photoetching allows the production of complex circuits (shift register, memories, multiplexing circuits, etc.) and makes it possible to make circuits associated with display matrices or teleprinter heads (read-out/restitution).

A process for making a restitution head for a teleprinter will be described by way of example.

It will be recalled that the electrosensitive paper which may be used in teleprinting may be classified in two families, the first grouping electrothermosensitive and metallized papers, and second grouping the electrolytic and electrocatalytic ones.

At the present time, only slow teleprinters (employing stylet) or alphanumerical printers are known for the first family; for the second family, no marketed apparatus exists.

To obtain a rapid teleprinter, of the same type as those which use (or which will use) heat-sensitive paper, a restitution head with multiple electrodes disposed in the form of a comb must be produced so that the mechanical displacements of the head are eliminated. There is then a problem of connection due to the very large number of connecting wires emerging from the head and the high definition of the electrodes, hence the necessity of multiplexing the latter. According to a known art, this multiplexing is obtained by associating a diode with each electrode.

Now, if, instead of heat-sensitive paper, an electrosensitive paper is used having a conducting base, the multiplexing circuits with diodes become unsuitable. It is no longer a diode which must be associated with each electrode, but a transistor, this considerably increasing the problems of connection.

It is an object of the present invention to solve this problem. To this end, the process used is characterized in that:

a row of electrodes (E_1, E_2 . . .) and two families of metal multiplexing channels (X_1, X_2 . . . and Y_1, Y_2 . . .

) parallel to one another and to said row, are deposited on an insulating substrate;

four primary layers, insulating, semiconducting, insulating and metallic, respectively, are deposited on this substrate by the operations of the first phase mentioned hereinbefore;

the operations of the second phase, are then effected, the photoetching operations being carried out so as to leave zones constituted by said four layers, these zones being disposed on the one hand opposite each electrode at the desired site for control transistors (zones P_1, P_2 . . .) and on the other hand at crossing sites located on the two families of metal channels on a level with the electrodes (zones Q_1, Q_2 . . . on the first family and R_1, R_2 . . . on the second);

the operations in accordance with those described hereinabove are carried out on zones P_1, P_2 . . . to obtain at each site a T.F.T., or T_1, T_2 . . .

during the operations of depositing the layer of contact metal of the T.F.T.s and of photoetching this layer, metal connecting channels are produced, connecting, for each T.F.T., the grid to one of the multiplexing channels of one of the families, the source to one of the channels of the other family and the drain to the electrode disposed opposite this T.F.T.

The restitution head shown in FIGS. **3** and **4**, in two slightly different embodiments, comprises read-in electrodes E_1, E_2 . . . connected to transistors T_1, T_2 . . . of T.F.T. type. Each of these transistors comprises a grid G, a source S and a drain D. The control circuit of these transistors comprises two families of metal channels the first formed by channels X_1, X_2 . . . and the second of channels Y_1, Y_2 . . . In the variant of FIG. **3**, the channels X_1, X_2 . . . are connected to the grids of the T.F.T.s and the channels Y_1, Y_2 . . . to the sources of said T.F.T.s. In the variant of FIG. **4**, the channels X_1, X_2 . . . are connected to the sources of the T.F.T.s and the channels Y_1, Y_2 . . . to the grids of said T.F.T.s.

The principle of functioning of these two variants of a restitution head is summarized in the two Tables I and II hereinafter, in which a "1" indicates the application of a control voltage to a channel and a "0" the absence of such a voltage. In these Tables, only a few electrodes are shown in the first column, the others being controlled in accordance with the same principle.

FIGS. **5***a* to **5***c* illustrate different steps of the process for manufacturing a restitution head according to the variant of FIG. **3**.

Electrodes E_1, E_2 . . . and metal multiplexing channels X_1, X_2 . . . and Y_1, Y_2, Y_3 . . . are deposited on an insulating substrate **10** (for example made of glass). This deposit may be effected by evaporation in vacuo using an electron gun. The material to be evaporated is, for example, gold deposited on a chromium adhering layer. The shape of the electrodes and channels is obtained by photoetching. The substrate then has the appearance of FIG. **5***a* where the dimensions and proportions have not been respected in order to render the drawing clearer. The contact studs and supply circuits have not been shown.

Four consecutive deposits (insulator/semiconductor-/insulator/metal) are then made on the whole substrate of FIG. **5***a*, in accordance with the technique described hereinbove.

A first photoetching of these layers is carried out so as to leave zones P_1, P_2, P_3 . . . at the site of the future T.F.T.s and zones Q_1, Q_2, Q_3 . . . on channels X_1, X_2 . . . level with the electrodes, and finally, zones R_1, R_2, R_3 . . . on channels Y_1, Y_2 . . . at the site of the future crossings on the multiplexing channels (FIG. **5***b*).

Transistors T_1, T_2, T_3 . . . are then made at the site of zones P_1, P_2, P_3 . . . , in accordance with the operations described hereinbefore (FIG. **5***c*).

In FIG. **6**, a transistor T is shown in plan view (a) and in section along bb' and along cc' (b and c respectively). The references used in this Figure are those of FIG. **1**: substrate **1**, first insulating layer **2**, semiconductor layer **3**, second insulating layer **4**, grid contact **23**, source contact **24**, and drain contact **25**.

The crossing zones Q_1, Q_2 . . . and R_1, R_2 . . . are intended to avoid the electrical contacts between the vertical connections and the horizontal multiplexing channels. Of course, these channels do not exist at the site where a multiplexing channel must be connected to a vertical connection. A crossing zone comprises, in accordance with FIG. **7**, on one of the conducting channels X or Y deposited on the substrate, three of the four layers deposited during the first phase, namely an insulating layer **2**, a semiconductor layer **3** and an insulating layer **4**. The upper metal layer **5** of the zones is eliminated at the moment of photoetching of the grid of the T.F.T.s. This therefore does not involve any additional operation. Of course, the semiconducting properties of the layer **3** play no role in this insulation structure.

The crossing zones advantageously have dimensions which slightly exceed the dimensions of the conducting channels which they are to insulate.

The connections between the transistors, the restitution electrodes and the appropriate control channels are obtained by deposits of metal layers made during the deposit of the metal layer intended for producing the contacts of the T.F.T.s (reference **21** in FIG. **2***g*) The final result is illustrated in FIG. **5***c*.

Thus, apart from the prior deposit of the multiplexing channels, the process for manufacturing the control circuit according to the ivention merely uses operations necessary for obtaining T.F.T.s and therefore does not involve any additional operation.

TABLE I

	Control					
Electrodes	X_1	X_2	Y_1	Y_2	Y_3	Y_4
E_1	1	0	0	1	1	1
E_2	1	0	1	0	1	1
E_5	0	1	0	1	1	1
E_6	0	1	1	0	1	1

TABLE II

	Control					
Electrodes	X_1	X_2	Y_1	Y_2	Y_3	Y_4
E_1	0	1	1	0	0	0
E_2	0	1	0	1	0	0
E_5	1	0	1	0	0	0
E_6	1	0	0	1	0	0

What is claimed is:

1. In a process for making thin film transistors on an amorphous substrate, the steps;

(A) in a first phase: of introducing the substrate in a deposition chamber, making on all this substrate, without contact with the outside atmosphere, a uniform deposit of four successive primary layers; a first layer of protective insulating material, a second layer of semiconductor material, a third

layer of insulating material, of smaller thickness than the first layer, and finally a fourth layer of a metal,

(B) and, in a second phase,

of withdrawing the substrate coated with these four layers from the deposition chamber, by a first photoetching operation through a first mask, two openings for each transistor are opened through the fourth layer of metal and the third layer of insulator, the metal part remaining between these two openings constituting the grid of the transistor, and

a layer of diffusing metal is deposited on the whole of the substrate, then, by selective chemical attack, this second metal is eliminated, this leaving, in the semiconductor, two conducting zones, one constituting the drain and the other the source of the transistor.

2. The process of claim 1, wherein, with the aid of a second mask, a photoetching is then effected of the semiconductor in order to separate the transistors from one another.

3. The process of claim 2, wherein a deposit of a thick insulator different from the insulator used for the first and the third layer is then made on the whole substrate, after which, with the aid of a third mask, a window is opened in this thick insulator opposite the grid, the drain and the source.

4. The process of claim 3, wherein a deposit is then made of a layer of contact metal on the whole substrate after which, with the aid of a fourth mask, this layer is photoetched in order to obtain a grid contact, a drain contact and a source contact.

5. A process for making a restitution head of a teleprinter comprising a row of electrodes connected to a multiplexed control circuit, comprising the steps of:

depositing on an insulating substrate a row of electrodes and two families of metal multiplexing channels parallel to one another and to said row,

making on all this substrate, without contact with the outside atmosphere, a uniform deposit of four successive primary layers; a first layer of protective insulating material, a second layer of semiconductor material, a third layer of insulating material, of smaller thickness than the first layer, and finally a fourth layer of a metal,

carrying out a photoetching operation being so as to leave zones constituted by said four layers, these zones being disposed on the one hand opposite each electrode at the desired site for control resistors and on the other hand at crossing sites located on the two families of metal channels on a level with the electrodes,

carrying out on said zones operations to obtain at each site a thin film transistor, these operations consisting in a first photoetching operation through a first mask, two openings for each transistor being opened through the fourth layer of metal and the third layer of insulator, the metal part remaining between these two openings constituting the grid of the transistor and in depositing a layer of diffusing metal on the whole of the substrate, then in selective chemical attacking of this metal for eliminating it, this leaving, in the semiconductor, two conducting zones, one constituting the drain and the other the source of the transistor, and

during the operations of depositing the layer diffusing metal layer of the thin film transistors, and of photoetching this layer, producing metal connecting channels connecting, for each transistor, the gate to one of the multiplexing channels of one of the families, the source to one of the channels of the other family and the drain to the electrode disposed opposite this transistor.

* * * * *